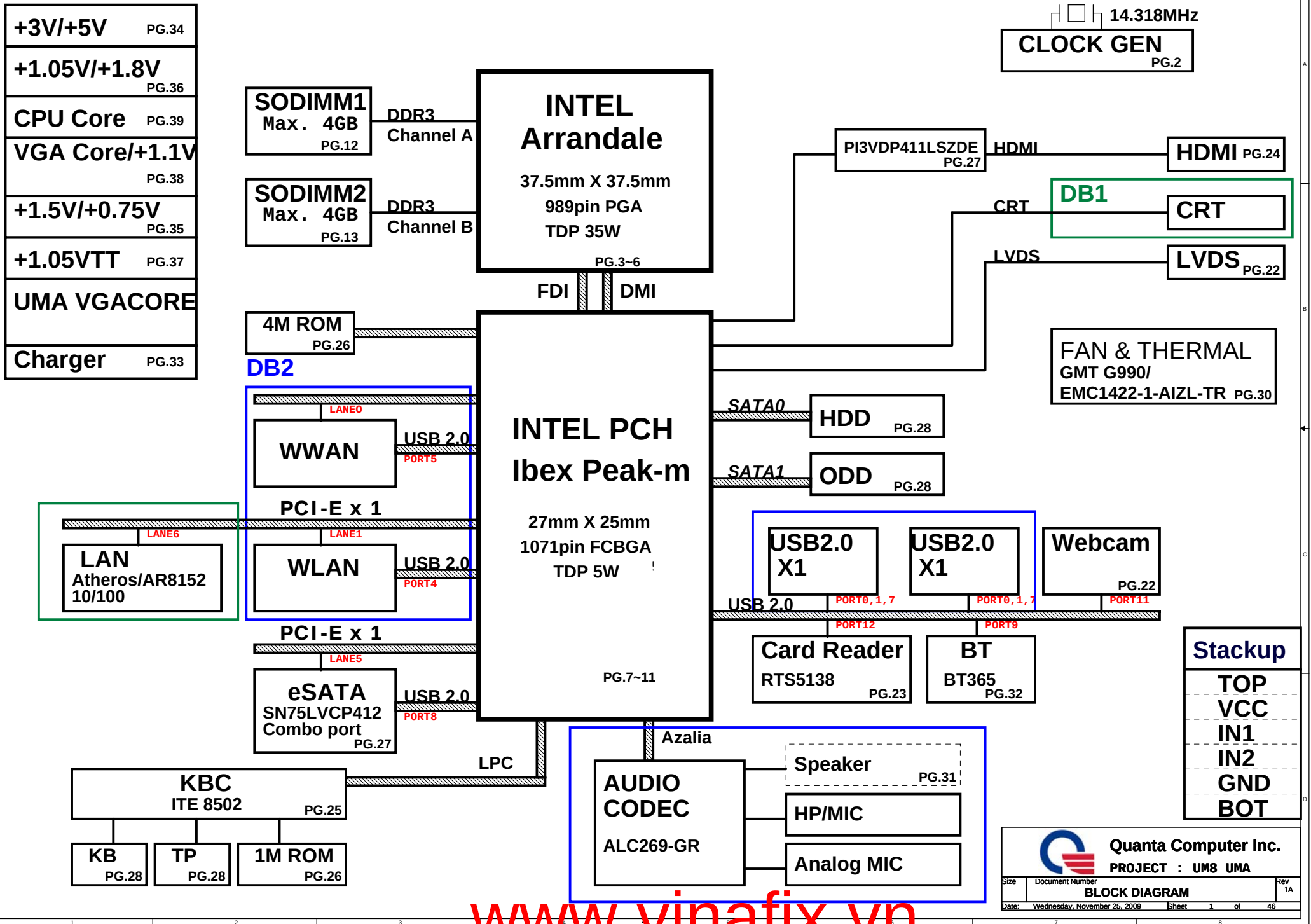
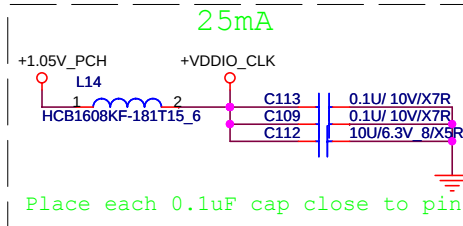
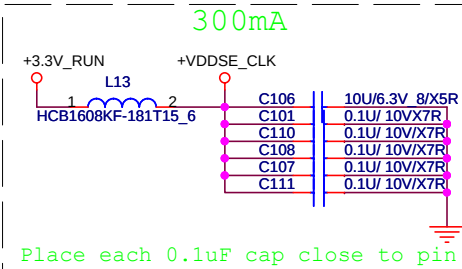


UM8 UMA SYSTEM DIAGRAM



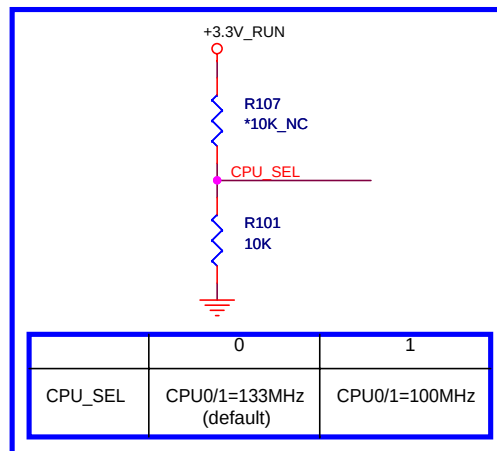
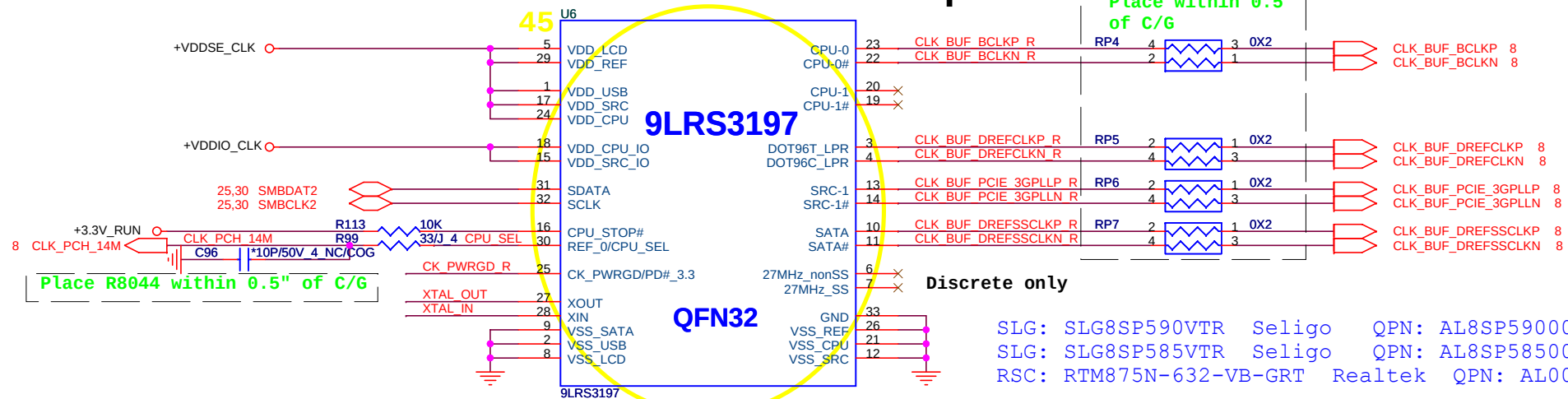


8/20 Wait Victor check

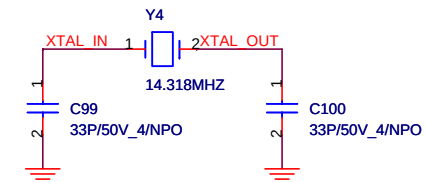
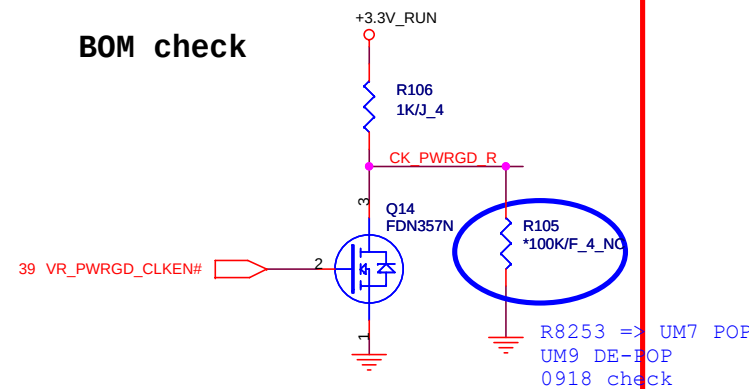


PDC (Power Cap quantities follow UM3)

Check CLK P/N and footprint



BOM check



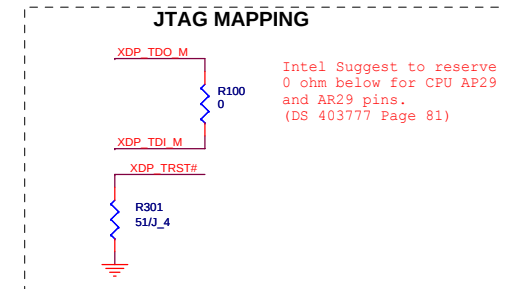
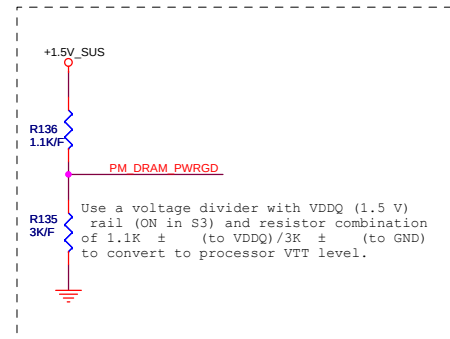
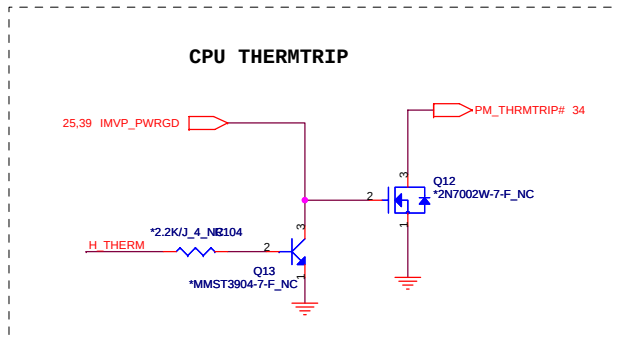
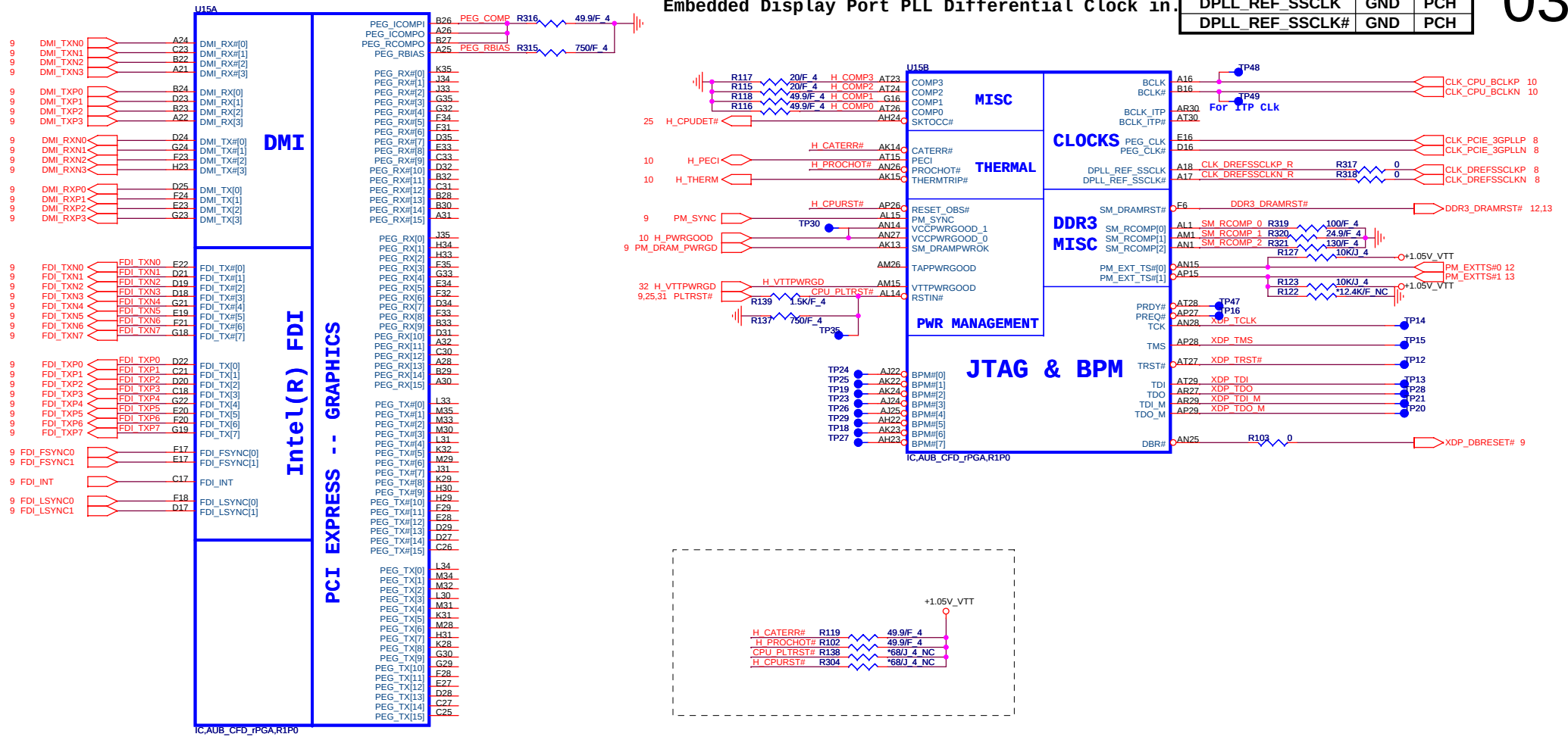
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Clock Gen(9LRS3197)/HOLES	Rev 1A
Date:	Wednesday, November 25, 2009	Sheet 2 of 46	

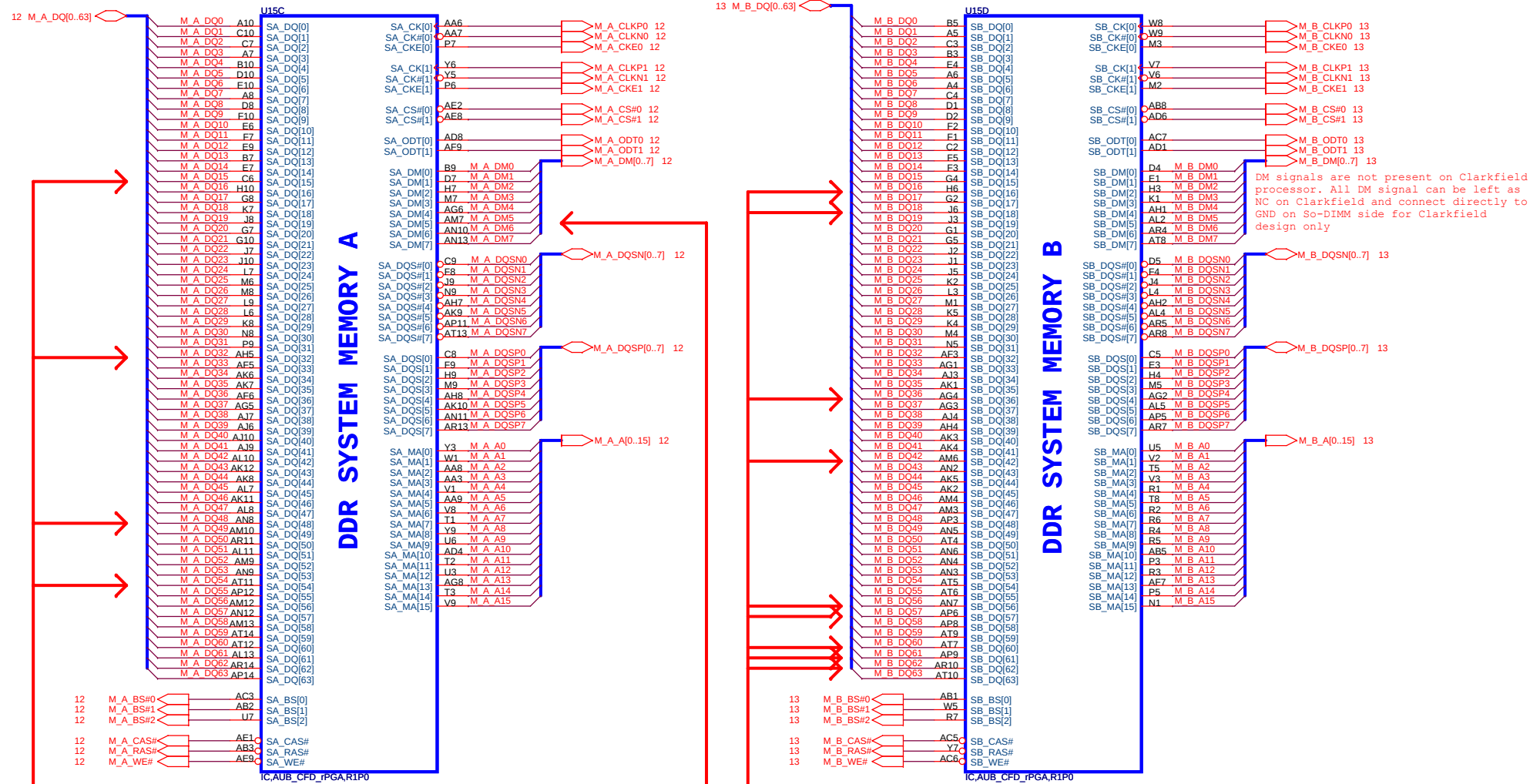
DPLL_REF_SSCLK/DPLL_REF_SSCLK#: Embedded Display Port PLL Differential Clock in.

DPLL_REF_SSCLK	DIS	UMA
DPLL_REF_SSCLK#	GND	PCH

03



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



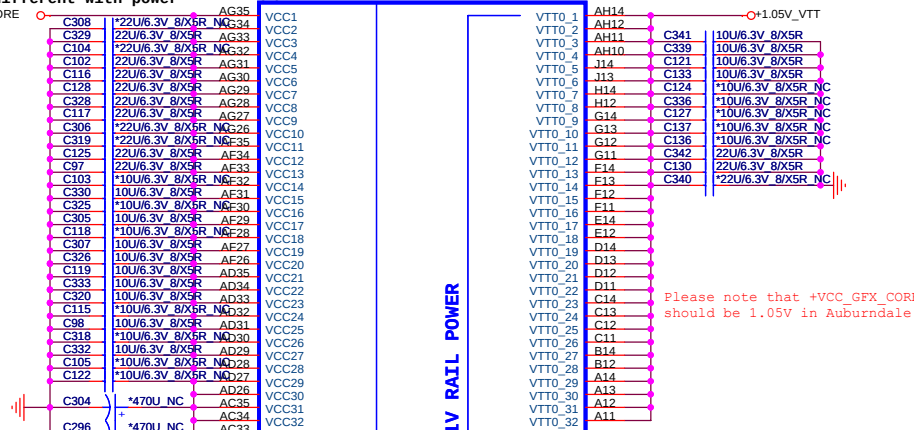
Name different with power

+VCC_CORE

U15F

18A

+1.05V_VTT



CPU CORE SUPPLY

POWER

1.1V RAIL POWER

CPU VIDS

SENSE LINES

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

VTT0_40

VTT0_41

VTT0_42

VTT0_43

VTT0_44

VTT0_33

VTT0_34

VTT0_35

VTT0_36

VTT0_37

VTT0_38

VTT0_39

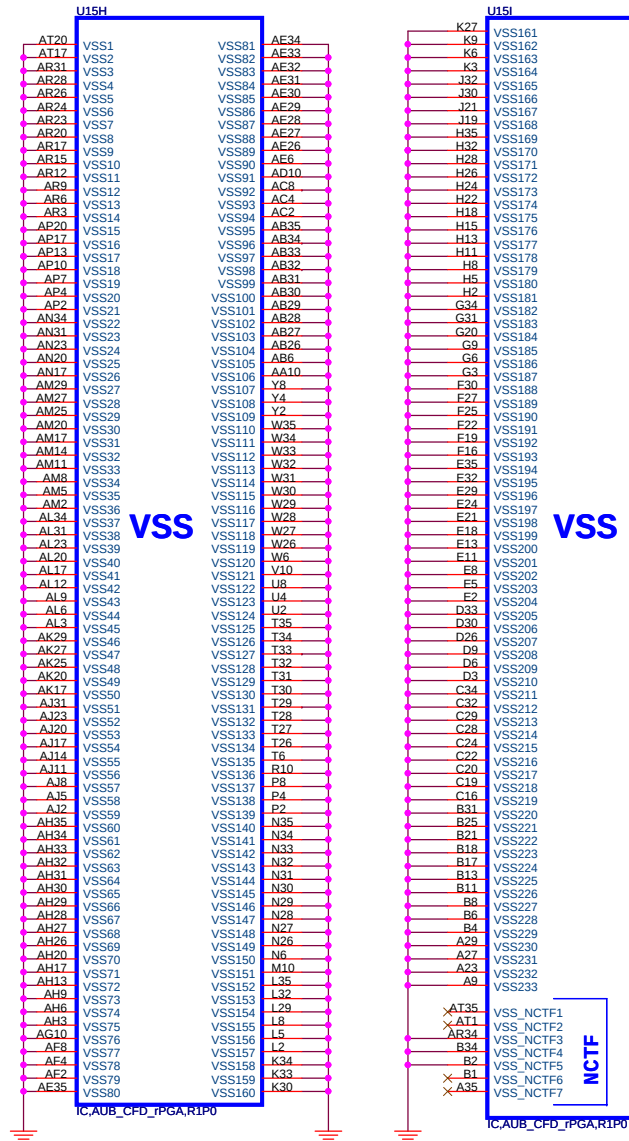
VTT0_40

VTT0_41

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

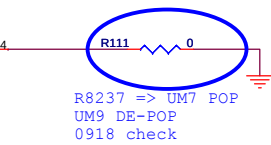
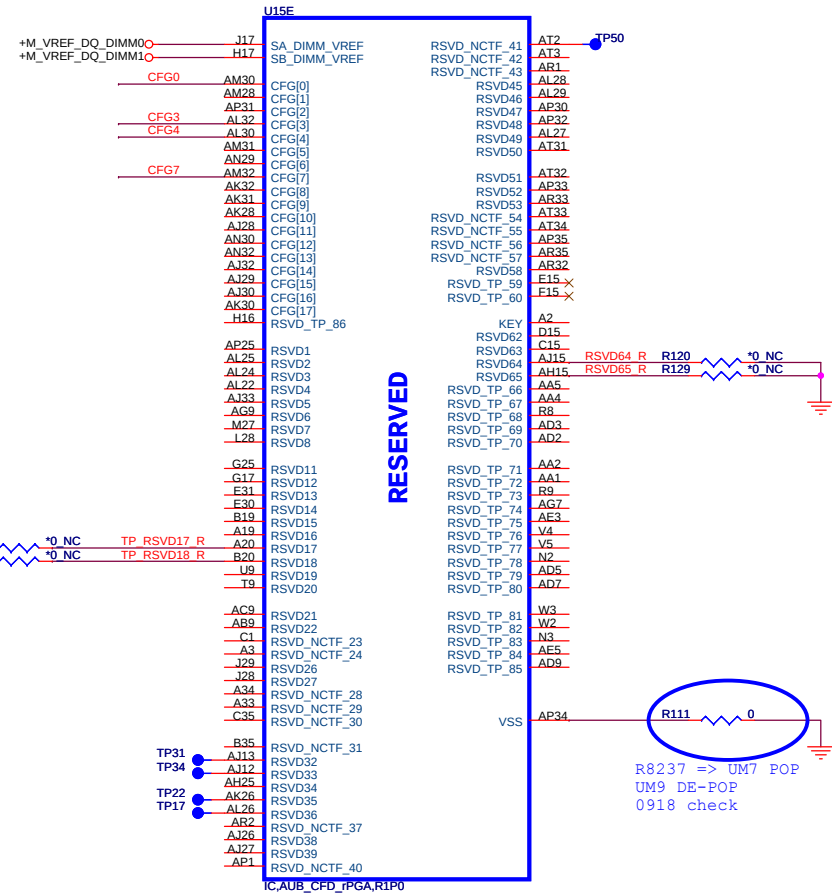
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

06

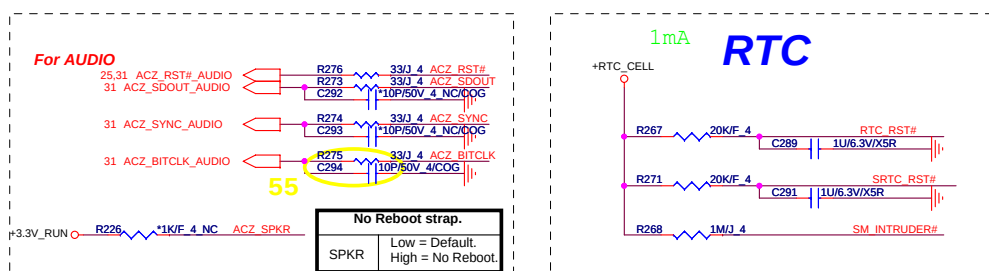
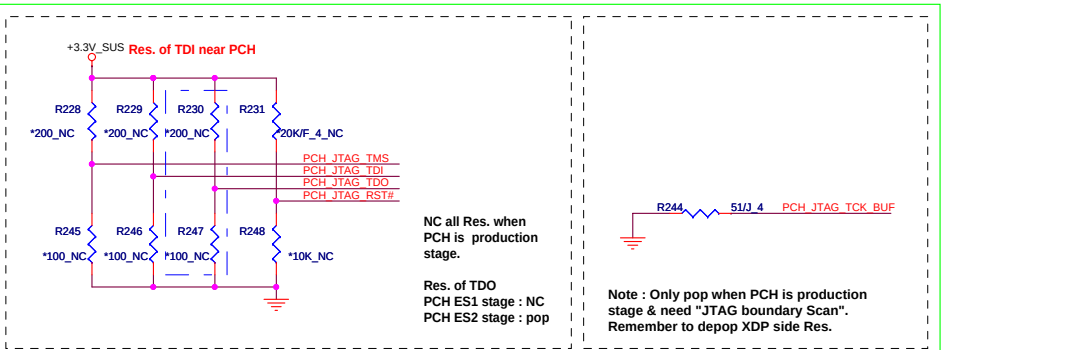
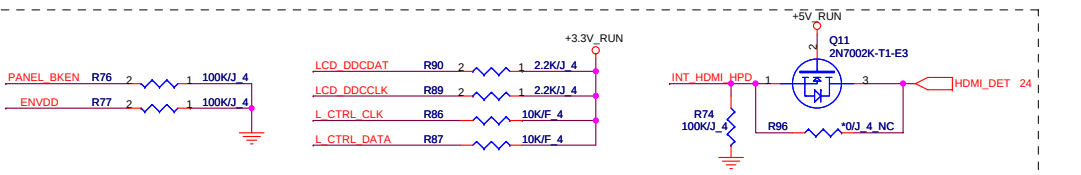


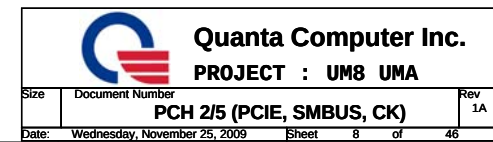
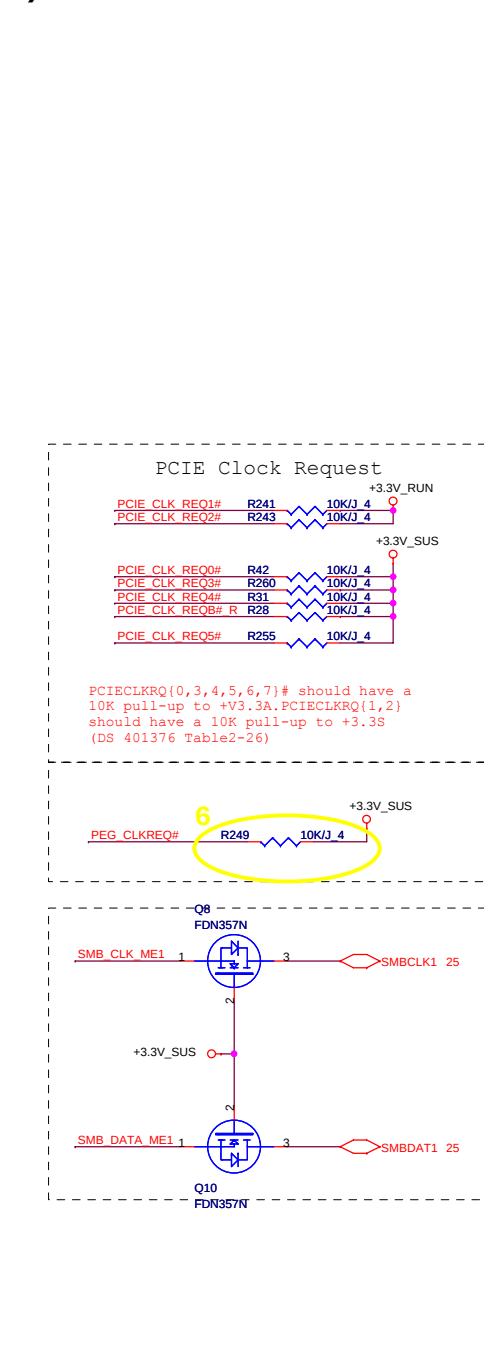
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

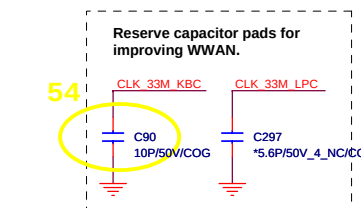
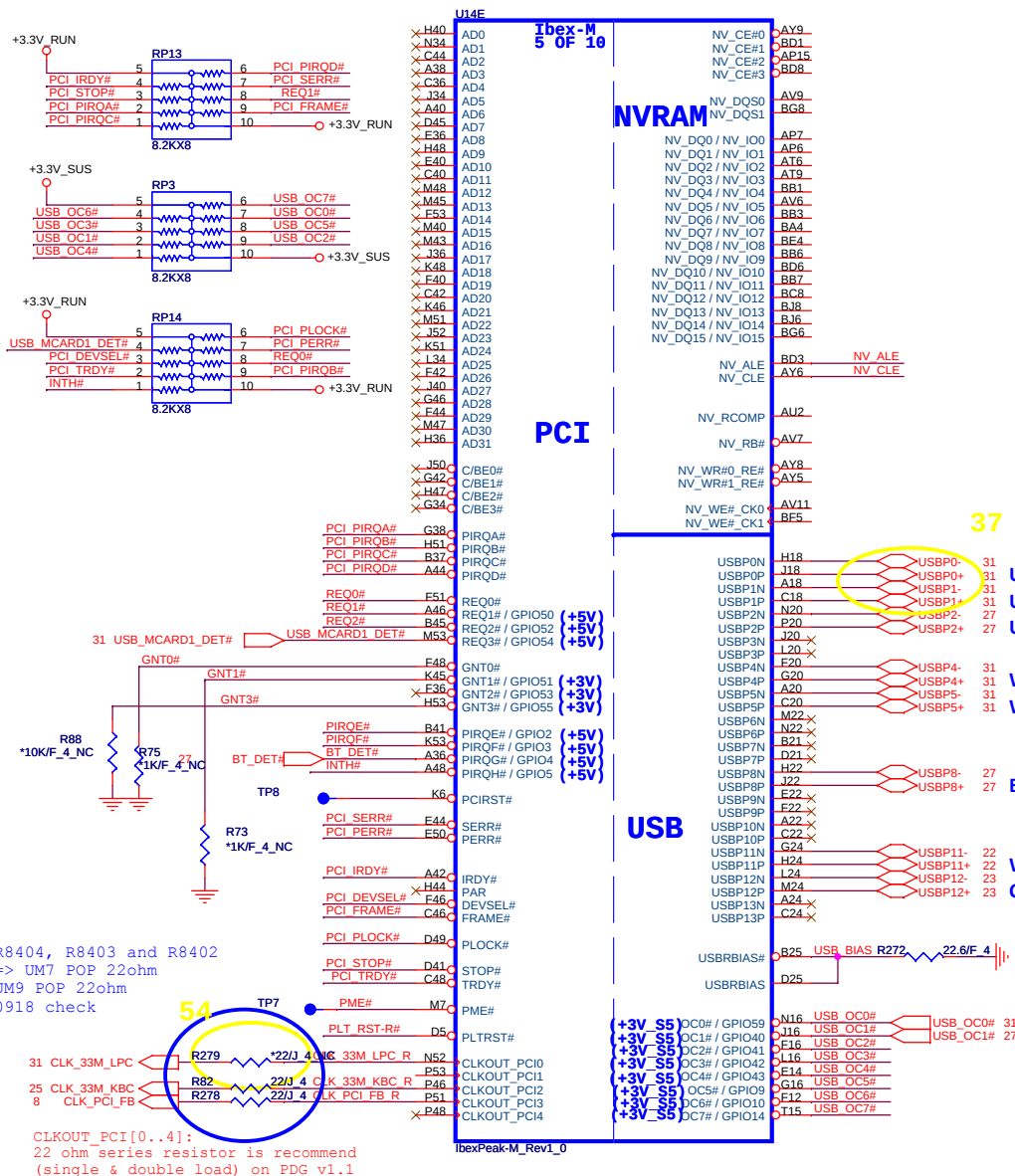


IBEX PEAK-M (HDA,JTAG,SATA)





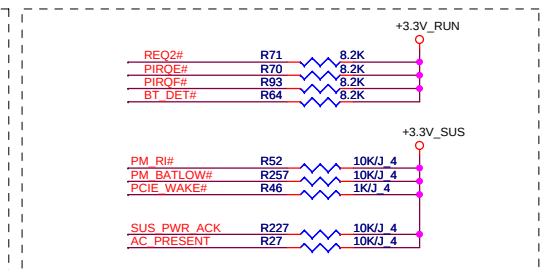
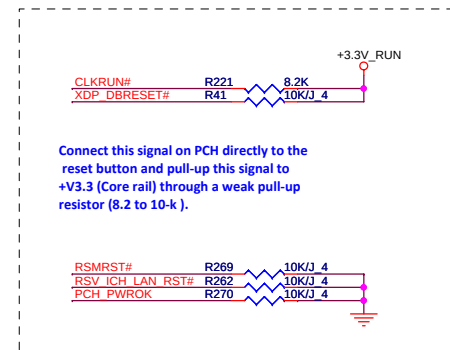
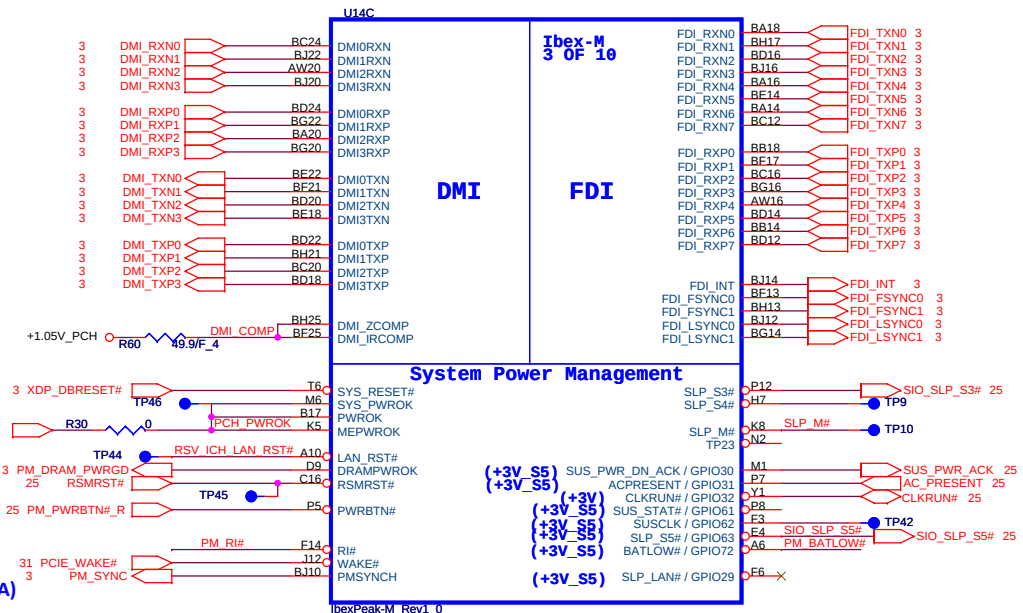
IBEX PEAK-M (PCI,USB,NVRAM)



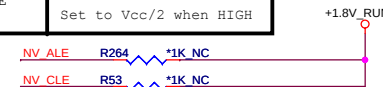
A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

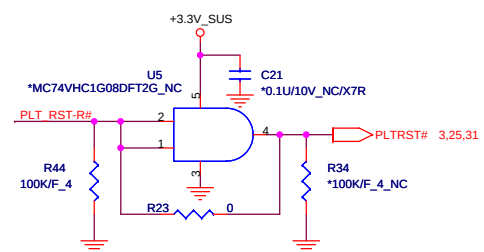
IBEX PEAK-M (DMI,FDI,GPIO)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH



Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

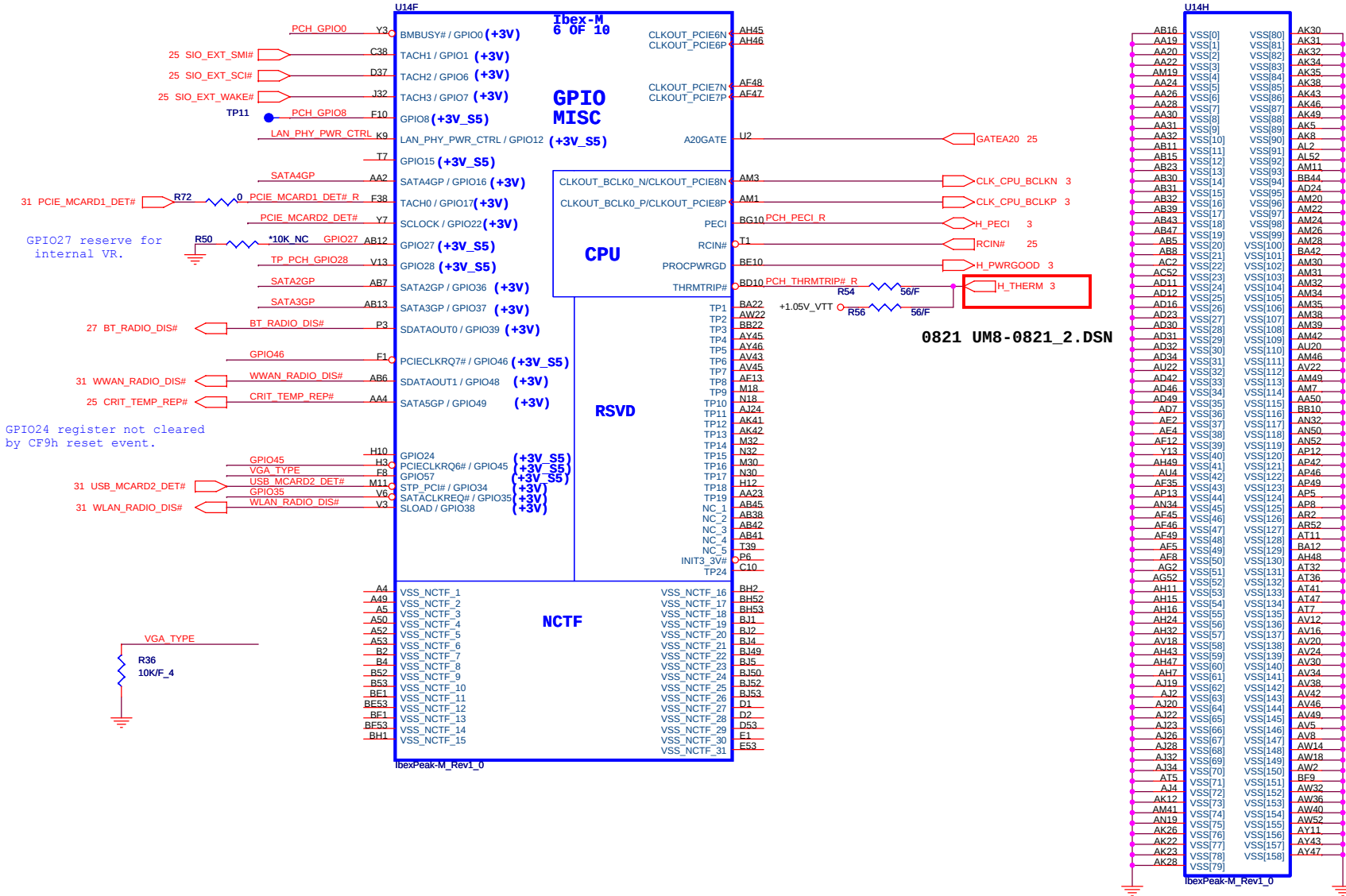


Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	1/
Date:	Wednesday, November 25, 2009	Sheet 9 of 46

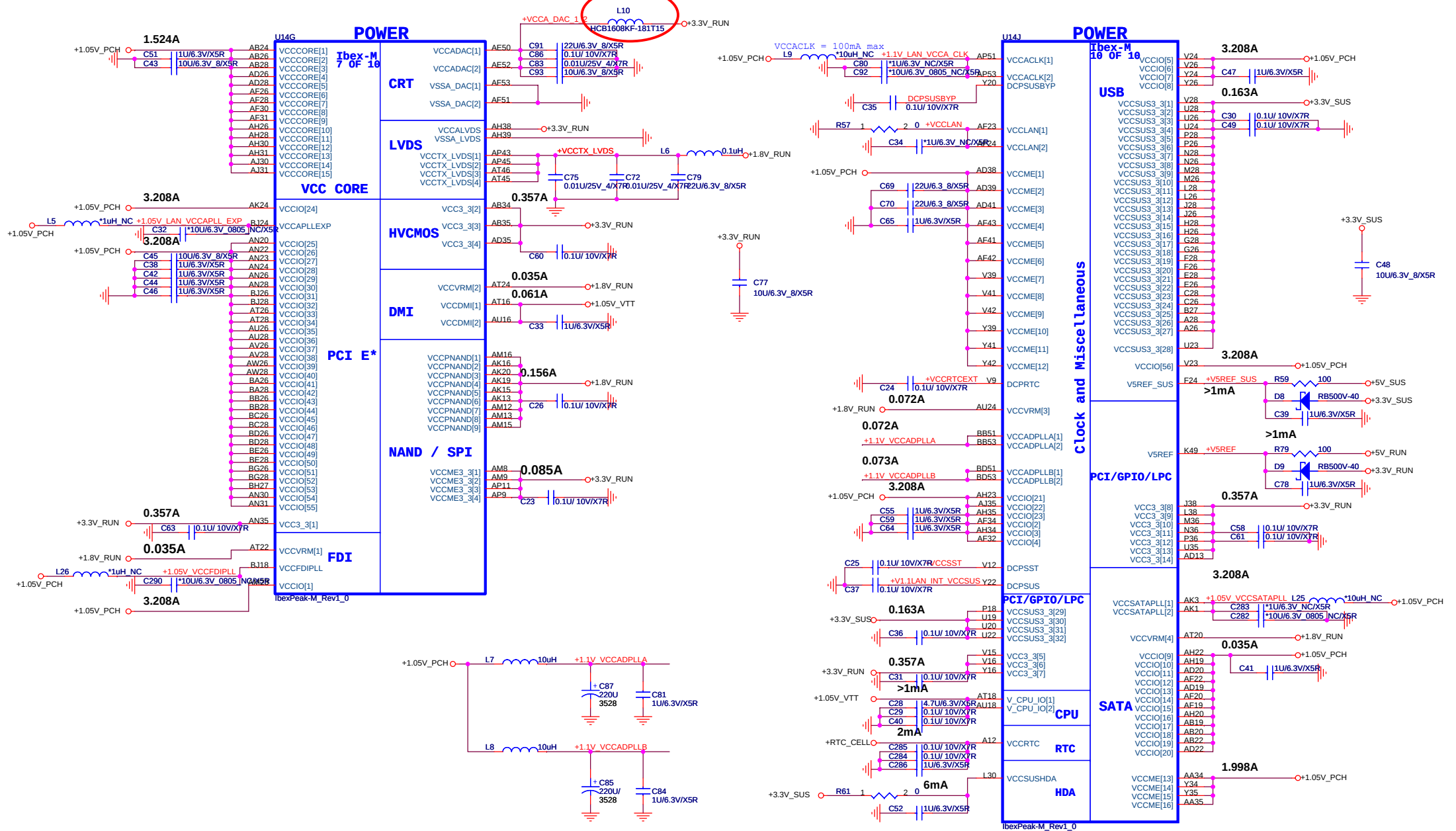
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

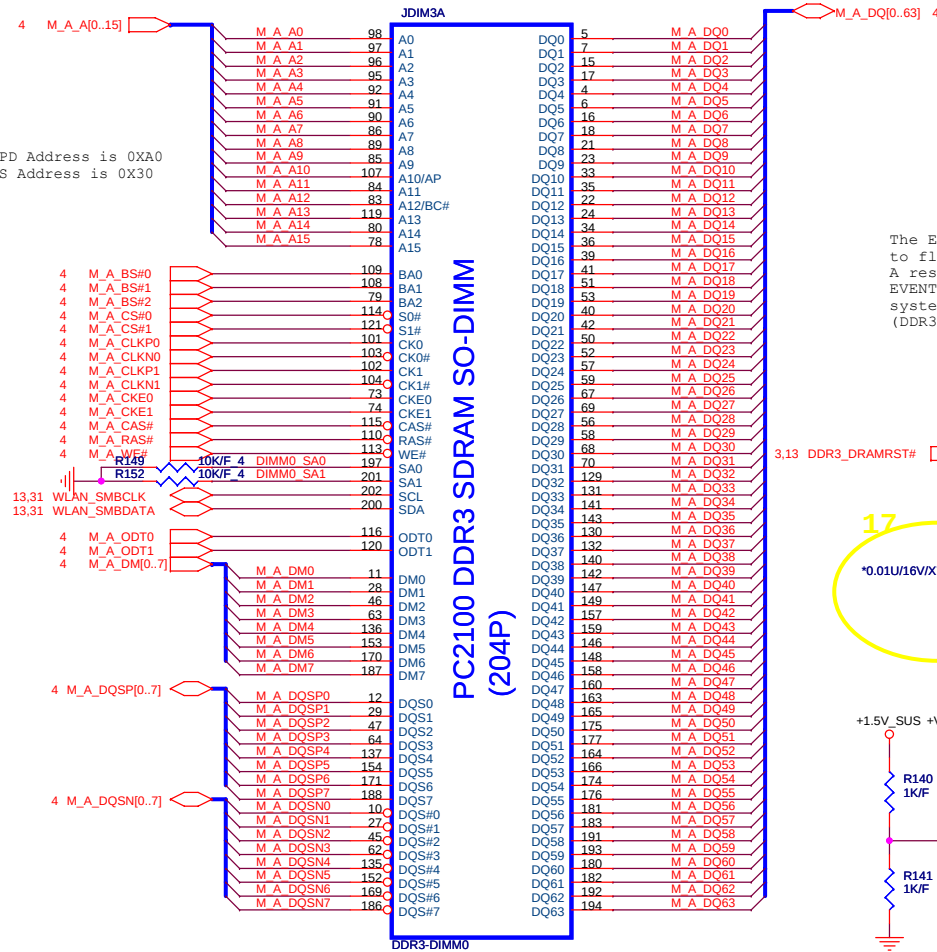


Cap quantities follow UM3

need check to change to 470 ohm



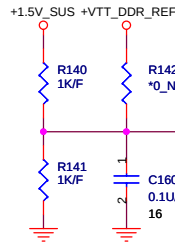
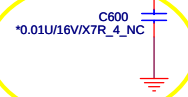
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30



The EVENT# pin is reserved for use to flag critical module temperature. A resistor may be connected from EVENT# bus line to Vddspd on the system planer to act as a pullup. (DDR3 DS REV0.5)

3.13 DDR3_DRAMRST#

17



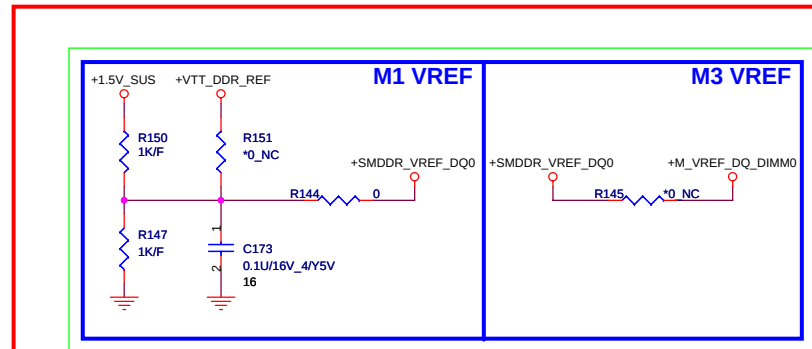
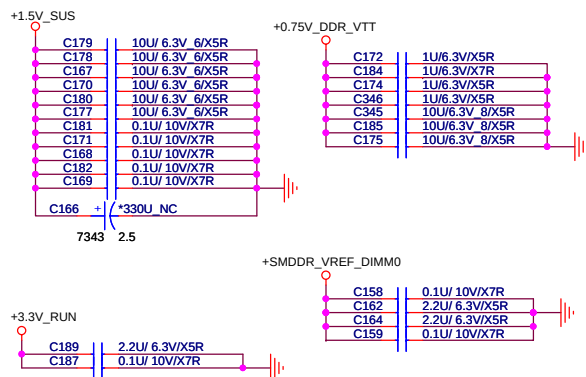
M2 VREF

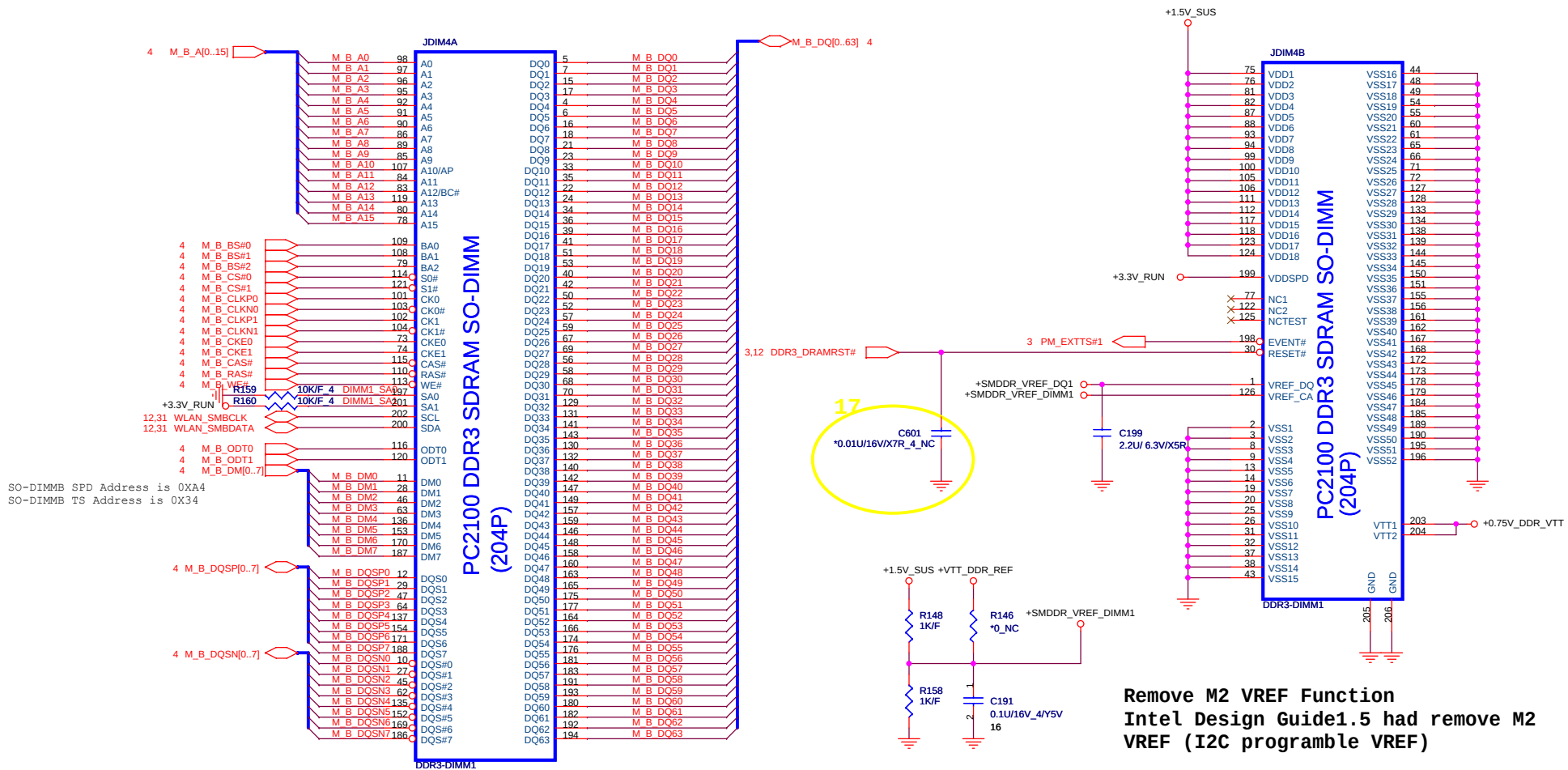
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

Place these Caps near So-Dimm0.

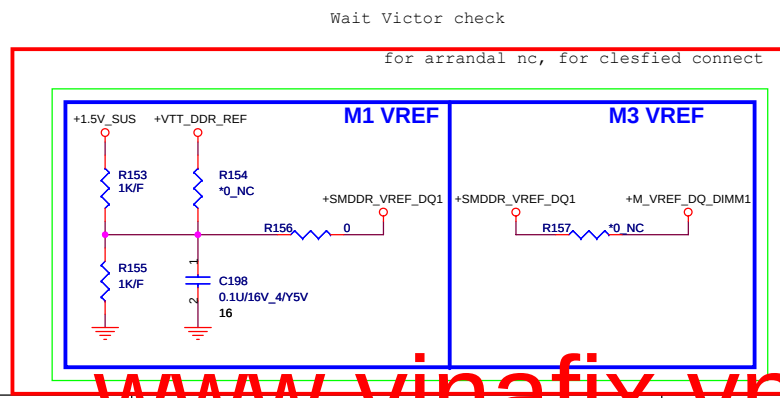
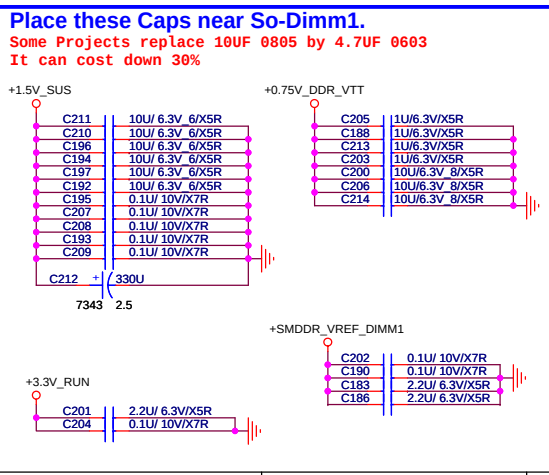
Some Projects replace 10uF 0805 by 4.7uF 0603
It can cost down 30%





Remove M2 VREF Function
 Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor





Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Blank	1A

Date: Wednesday, November 25, 2009 Sheet 15 of 46

	5	4	3	2	1
D					
C					
B					
A					

	5	4	3	2	1
D					
C					
B					
A					

	5	4	3	2	1
D					
C					
B					
A					

	5	4	3	2	1
D					
C					
B					
A					

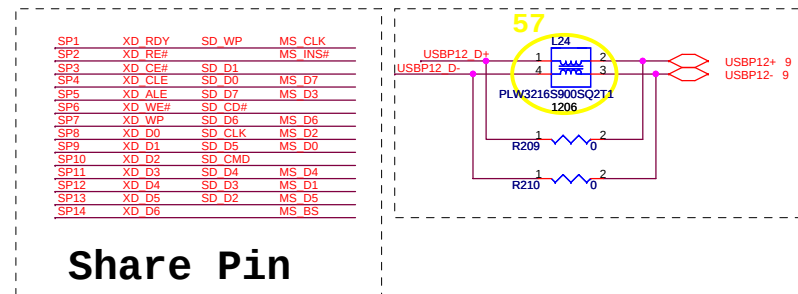
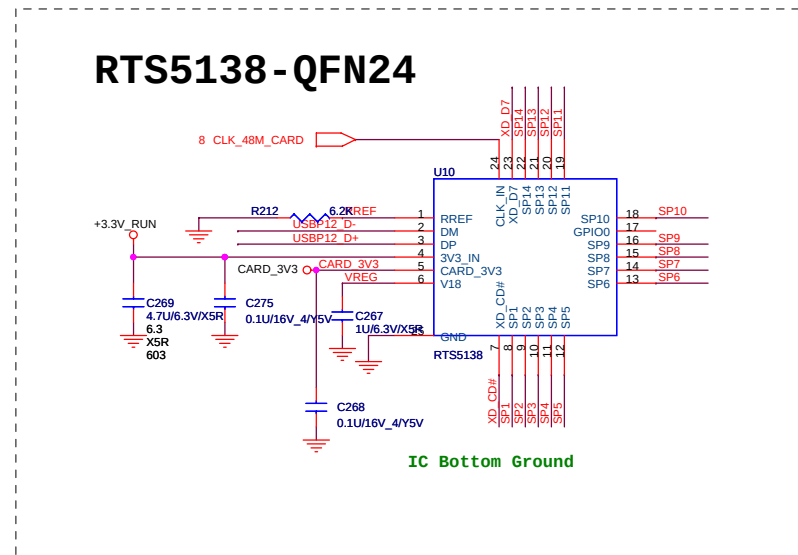
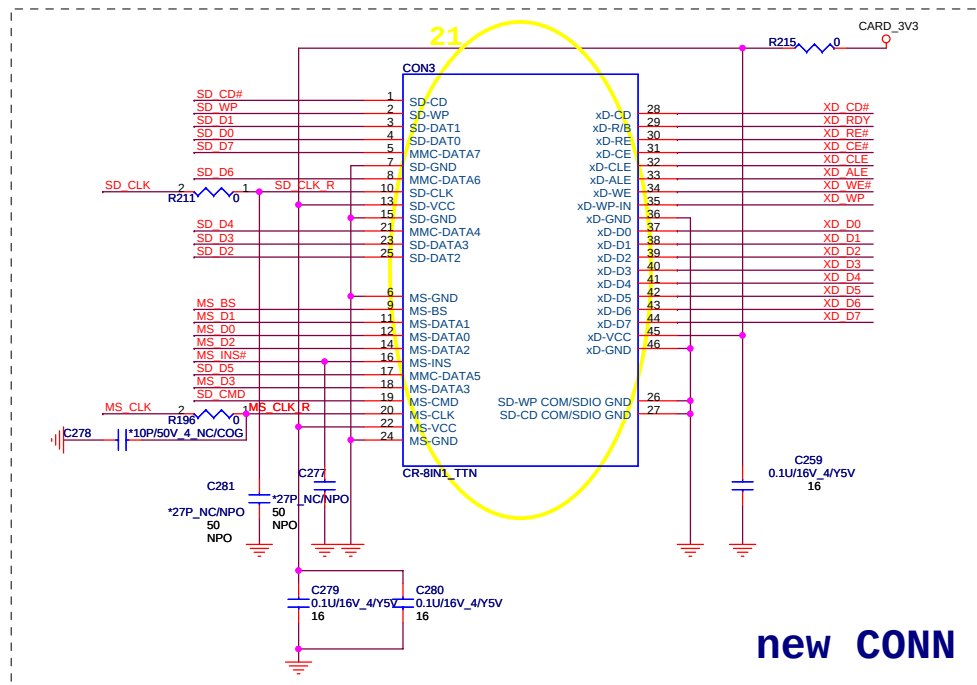


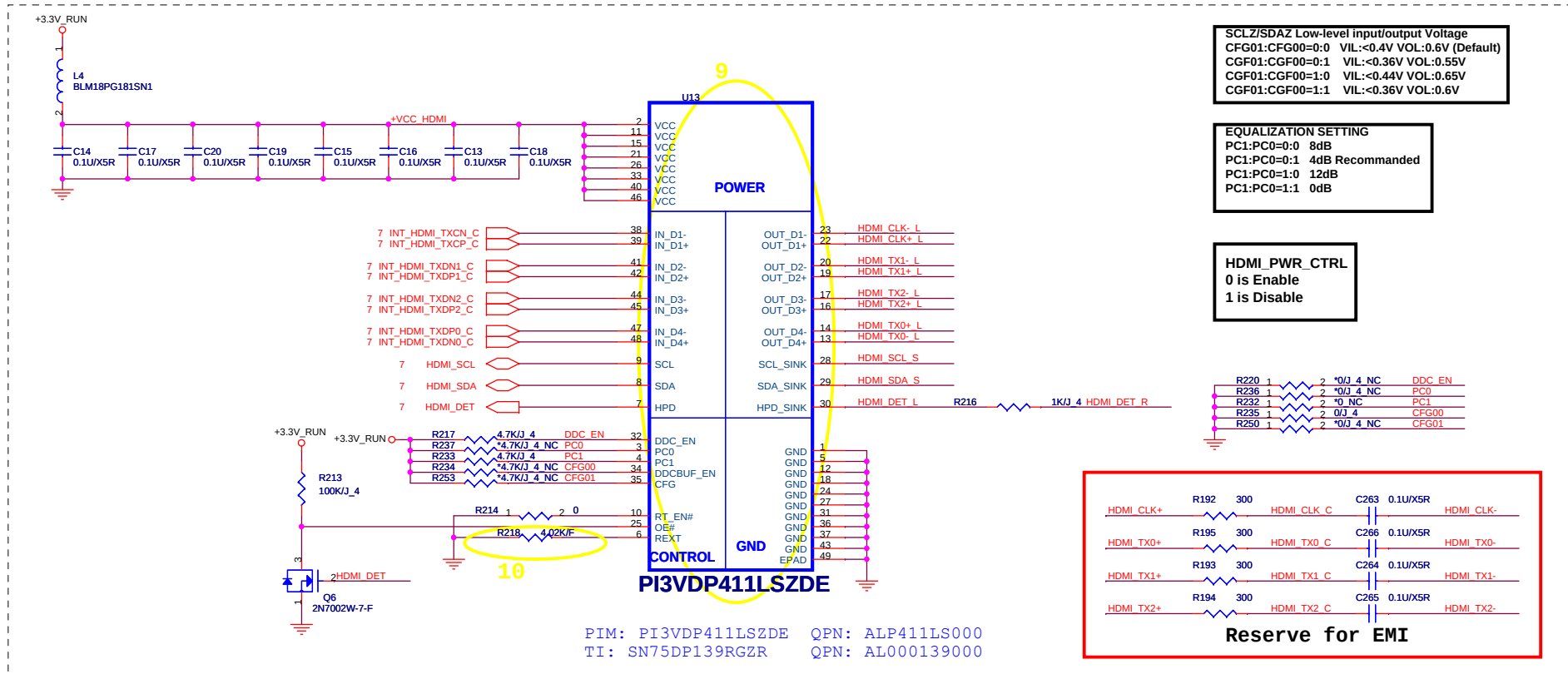
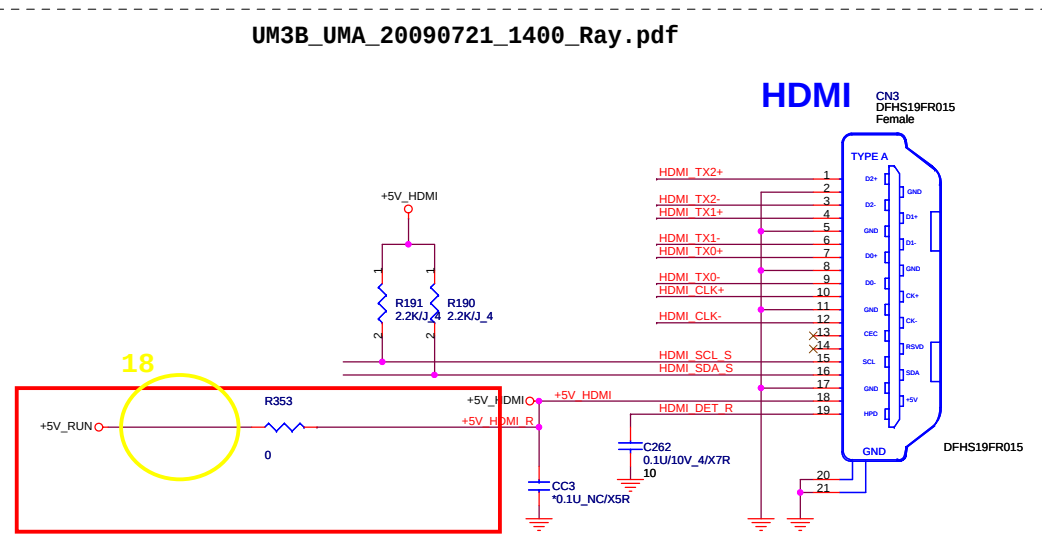
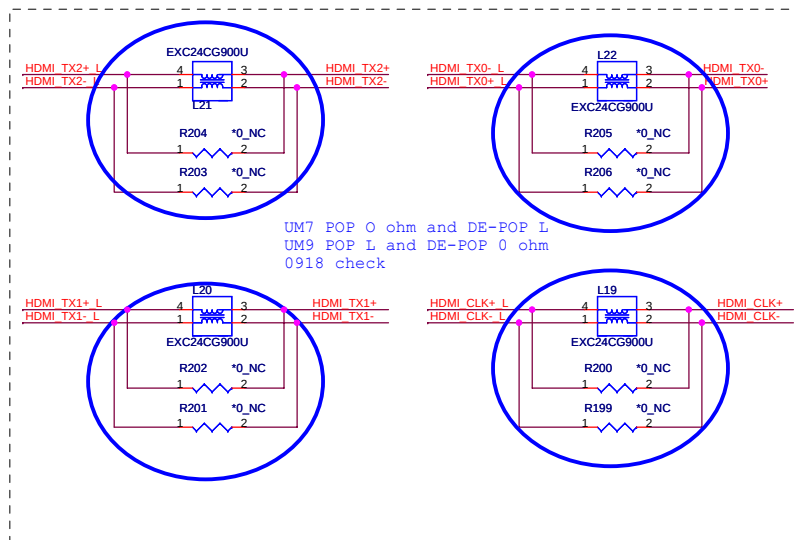
Quanta Computer Inc.

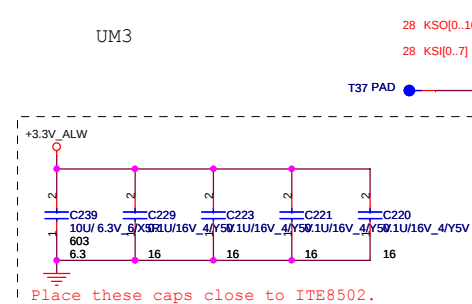
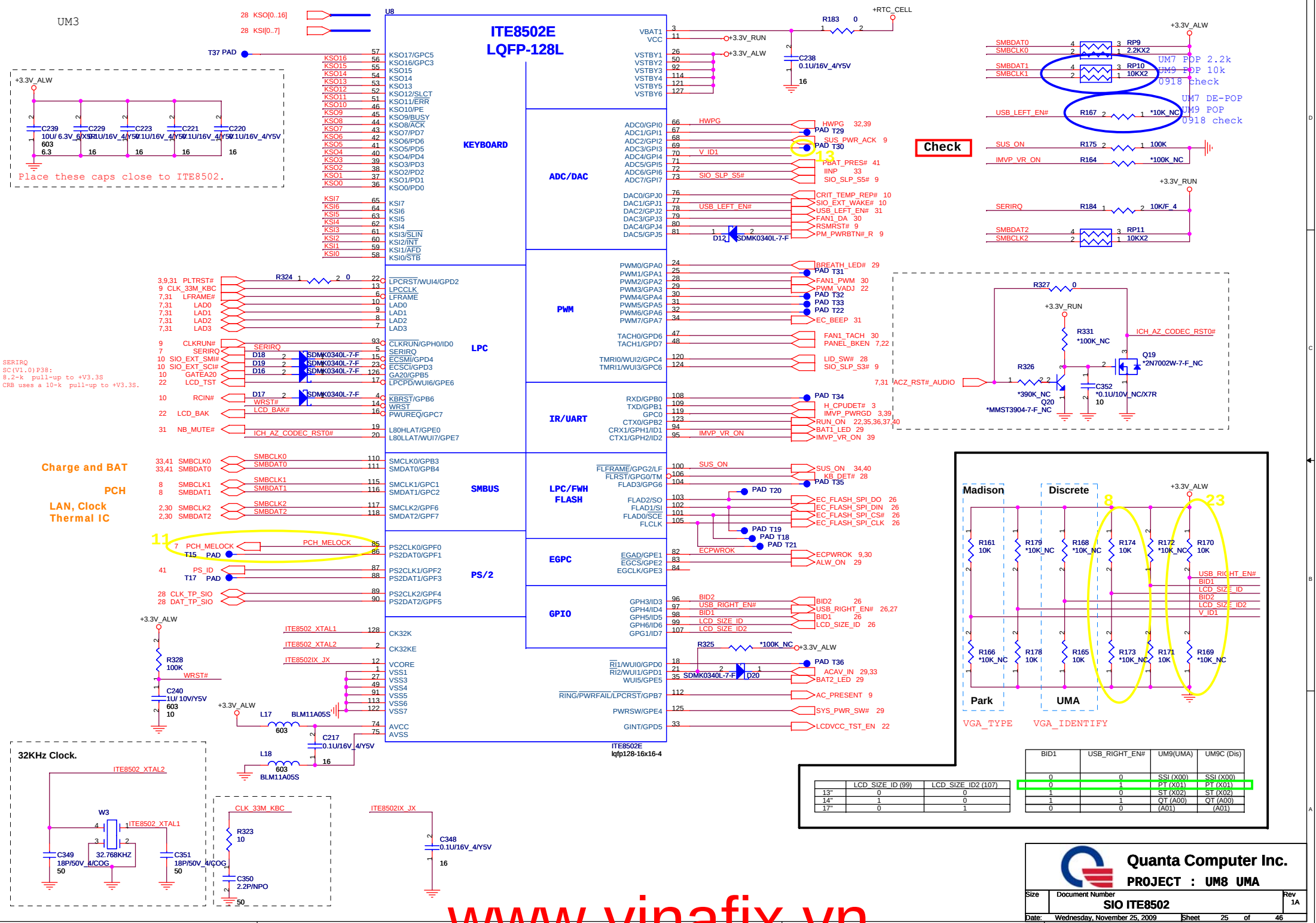
Size	Document Number	Rev
	Blank	1A

Date: Wednesday, November 25, 2009 Sheet 21 of 46

www.vinafix.vn



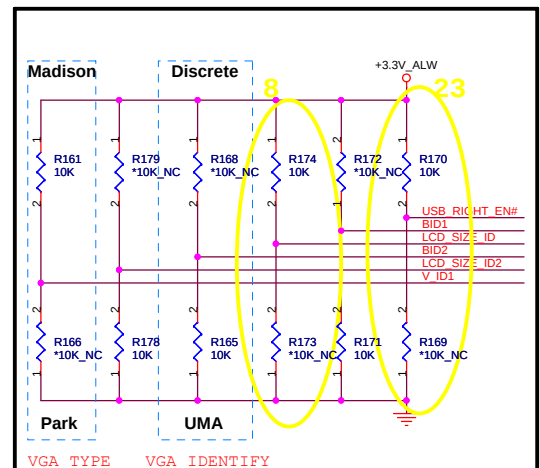
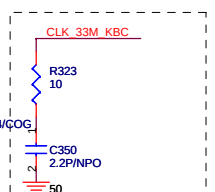
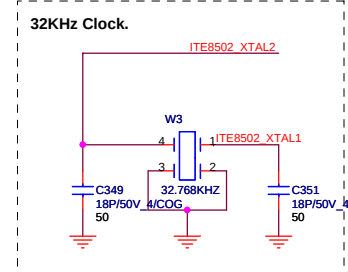




Place these caps close to ITE8502.

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Charge and BAT
PCH
LAN, Clock
Thermal IC



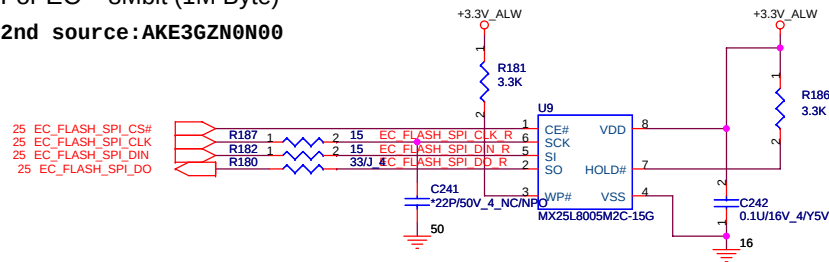
BID1	USB_RIGHT_EN#	UM9(UMA)	UM9C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	A01	A01

	LCD_SIZE_ID(99)	LCD_SIZE_ID2(107)
13"	0	0
14"	1	0
17"	0	1

UM3

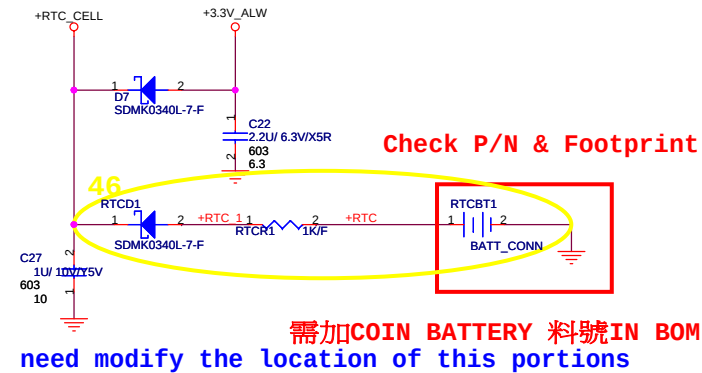
For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



MACRONIX: MX25L3205DM2I-12G QPN: AKE39FP0Z00
WINBOND: W25X32VSSIG QPN: AKE39ZP0N00

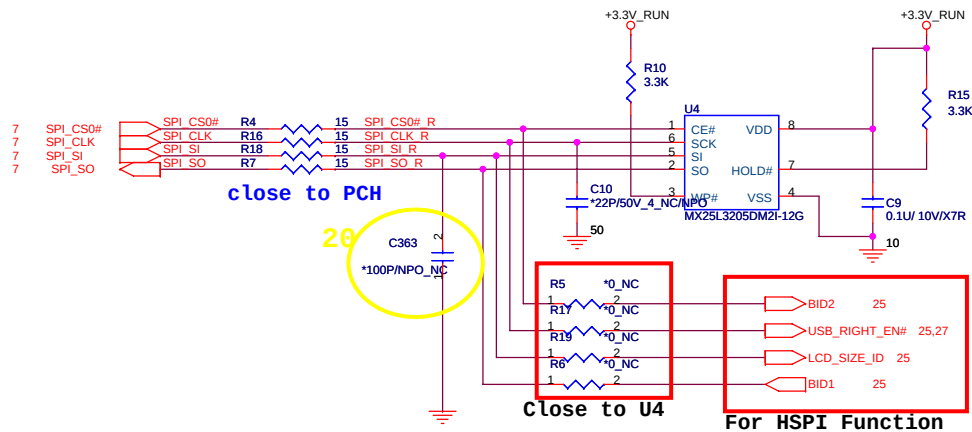
RTC BATTERY



For PCH

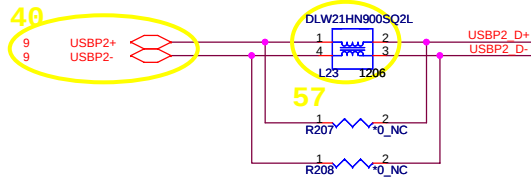
32Mbit (4M Byte)

MACRONIX: MX25L8005M2C-15G QPN: AKE5GFK0Z09
WINBOND: W25X80AVSSIG QPN: AKE39ZP0N00



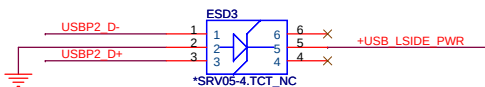
eSATA and USB To DB

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

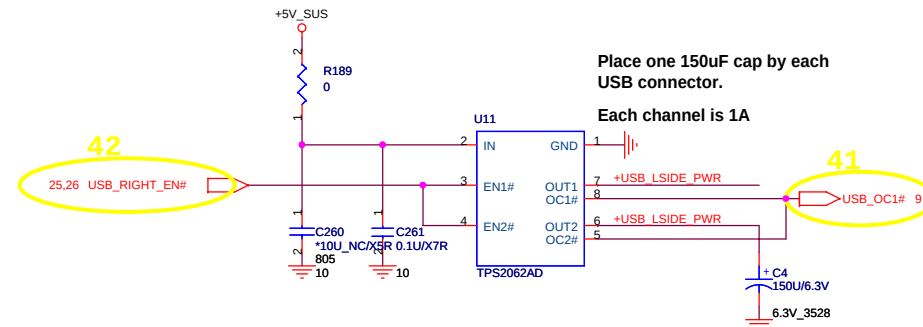
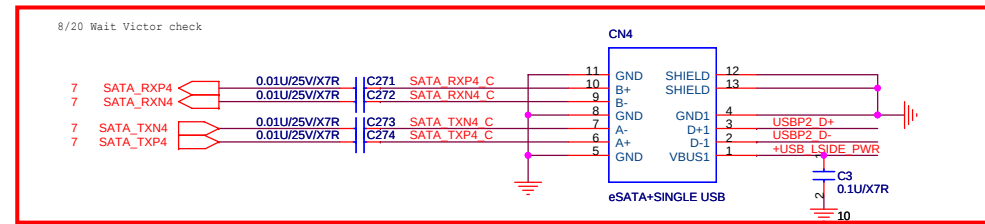


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

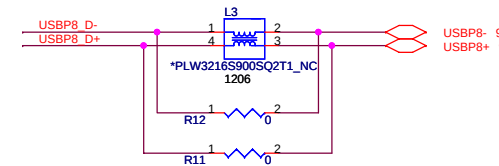
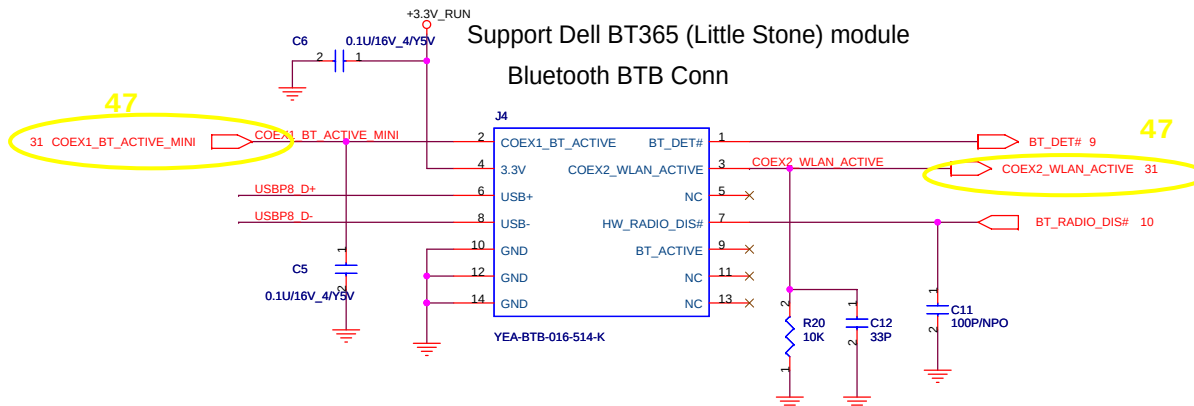
Place ESD diodes as close as USB connector.



USB and eSATA Conn.



Support Dell BT365 (Little Stone) module Bluetooth BTB Conn

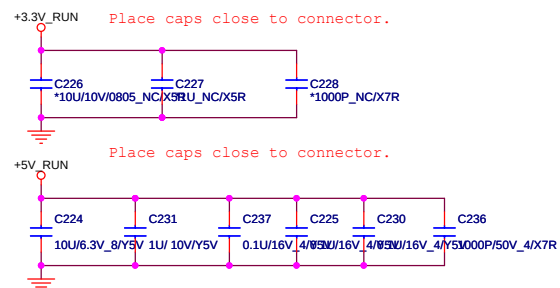
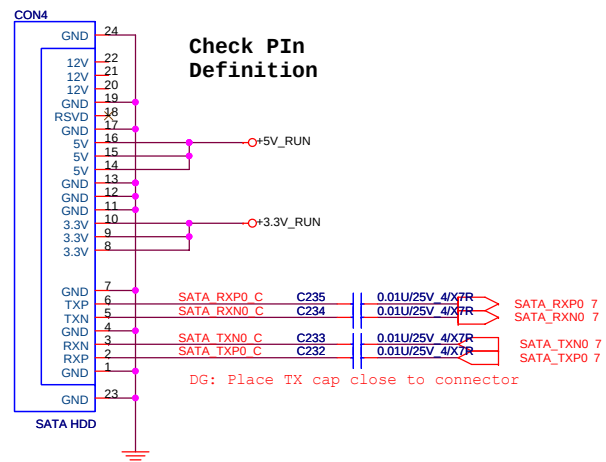


Quanta Computer Inc.
PROJECT : UM8 UMA

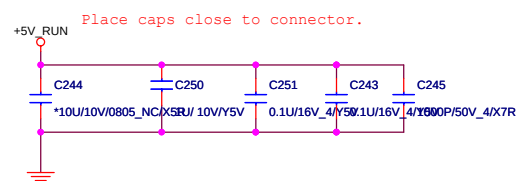
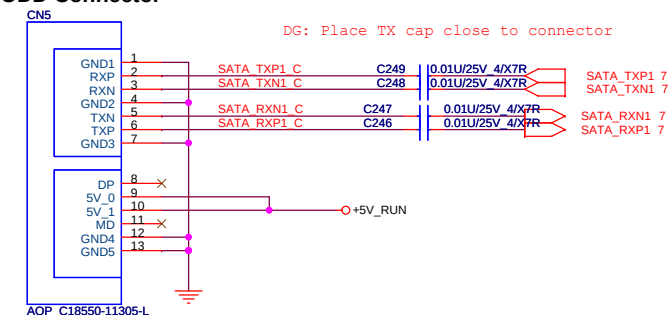
Size Document Number eSATA & Right USB
Date: Wednesday, November 25, 2009 Sheet 27 of 46 Rev 1A

www.vinafix.vn

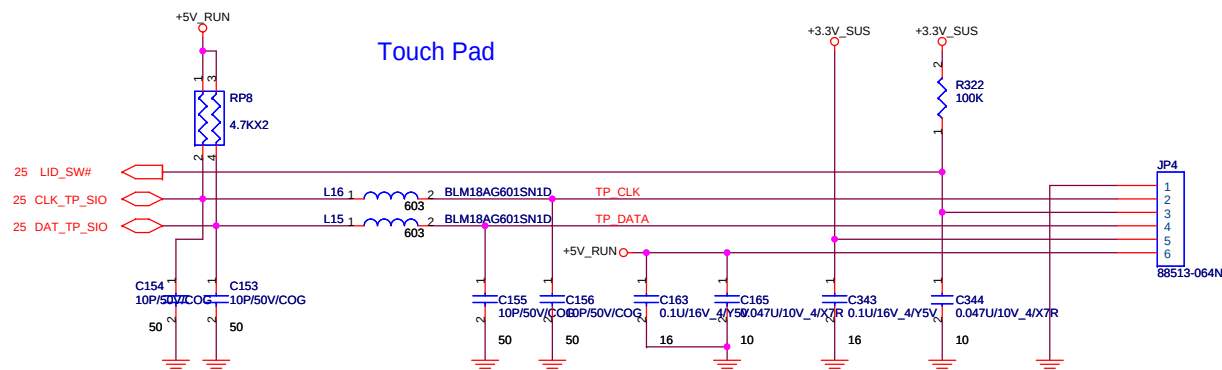
SATA Connector.



ODD Connector

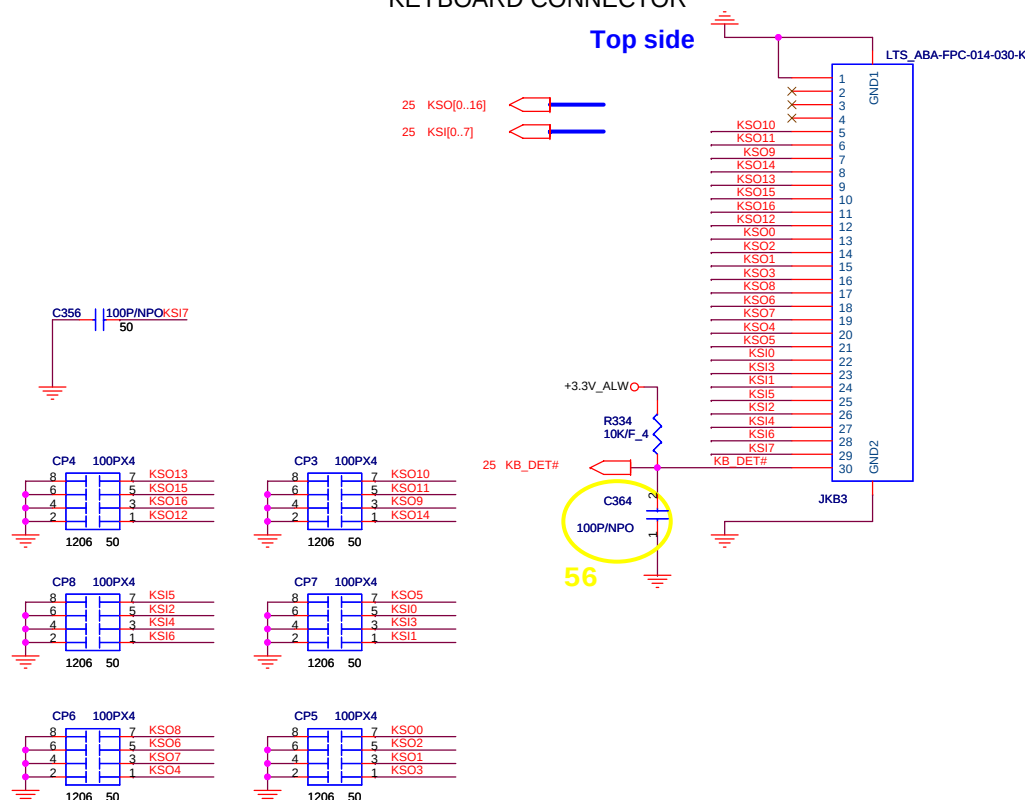


Touch Pad



KEYBOARD CONNECTOR

Top side



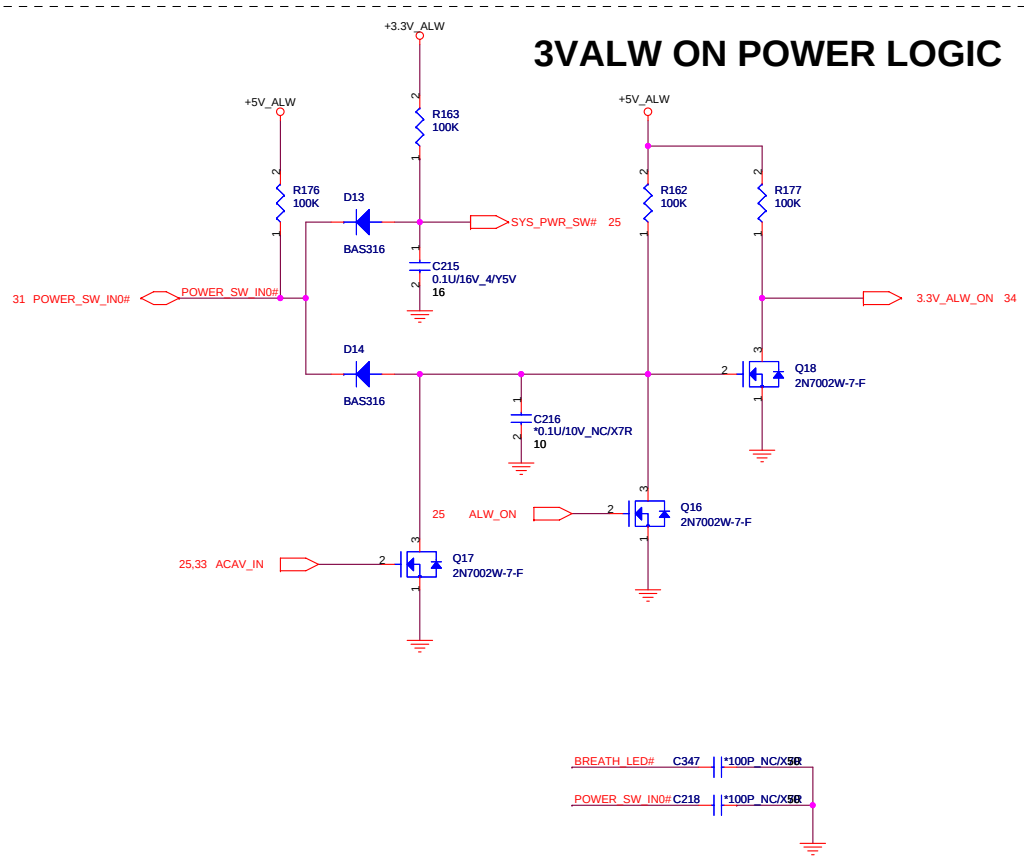
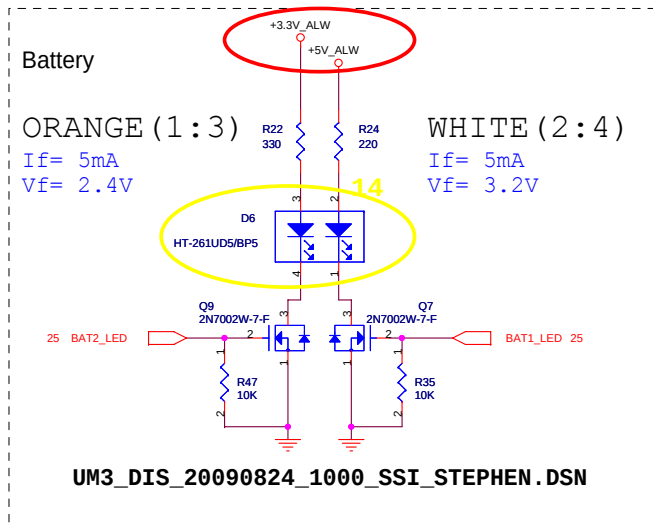
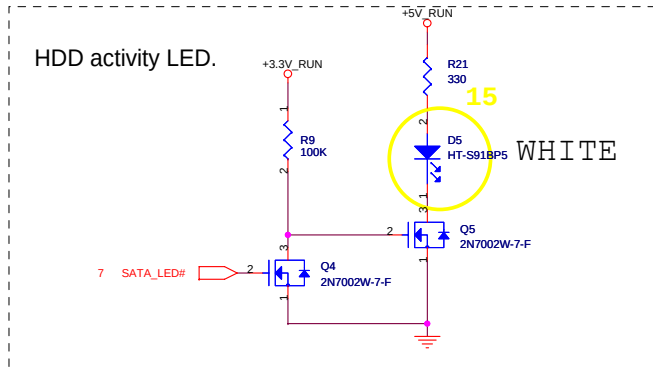
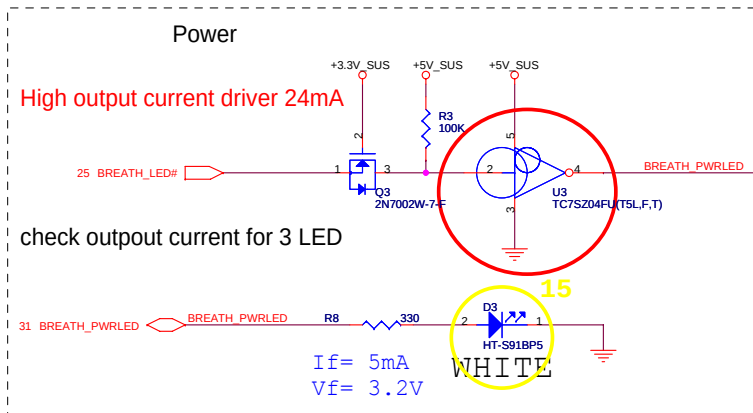
100P CAPS CLOSE TO JKB1

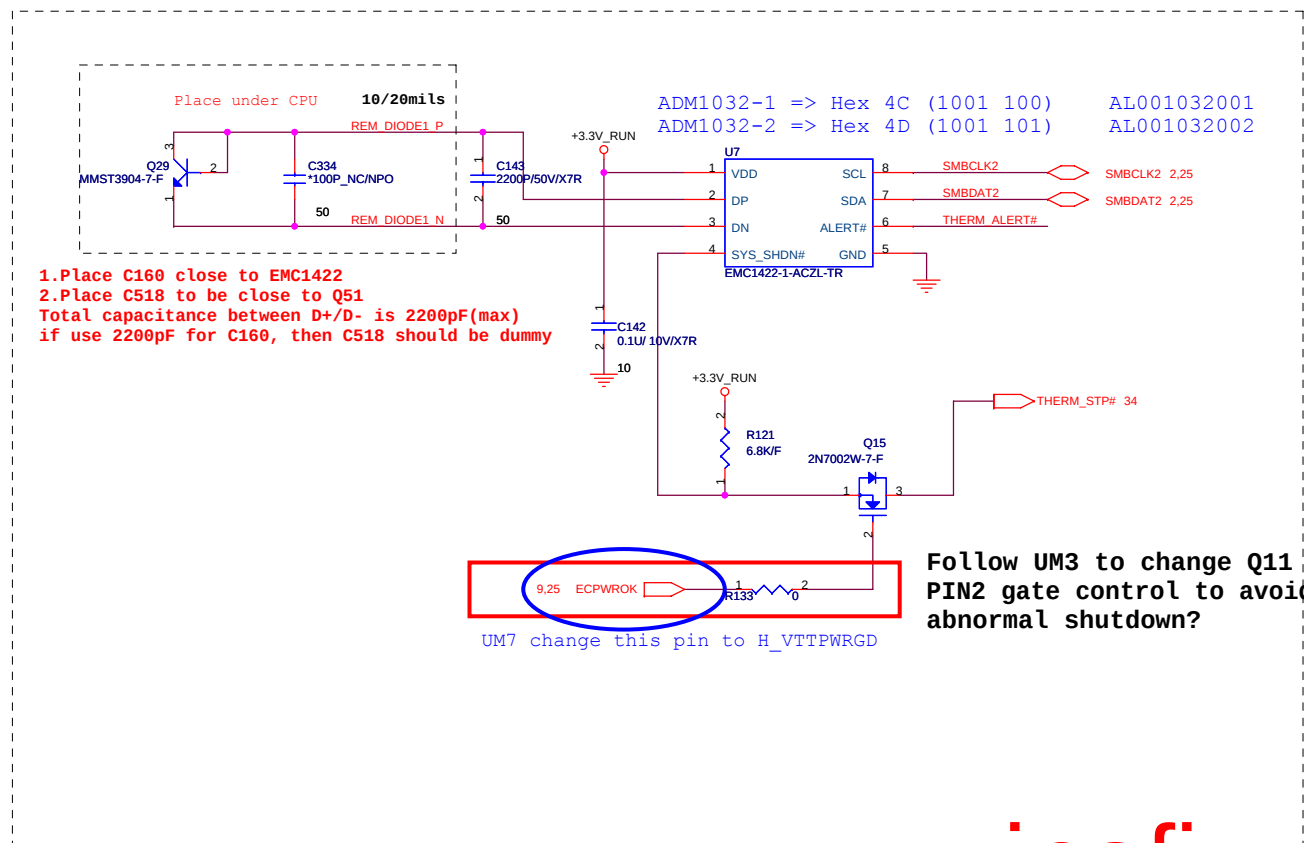


Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	SATA (HDD&ODD) & TP & KB	1A
Date:	Wednesday, November 25, 2009	Sheet 28 of 46

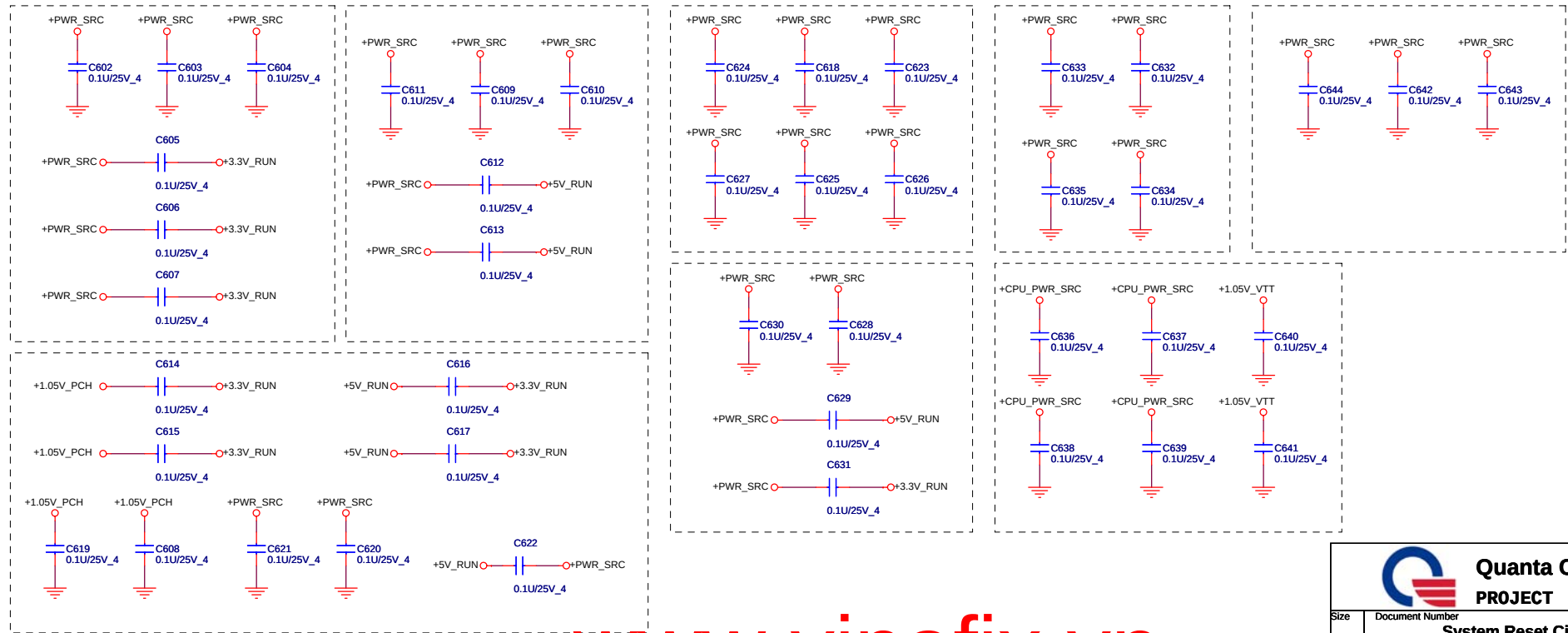
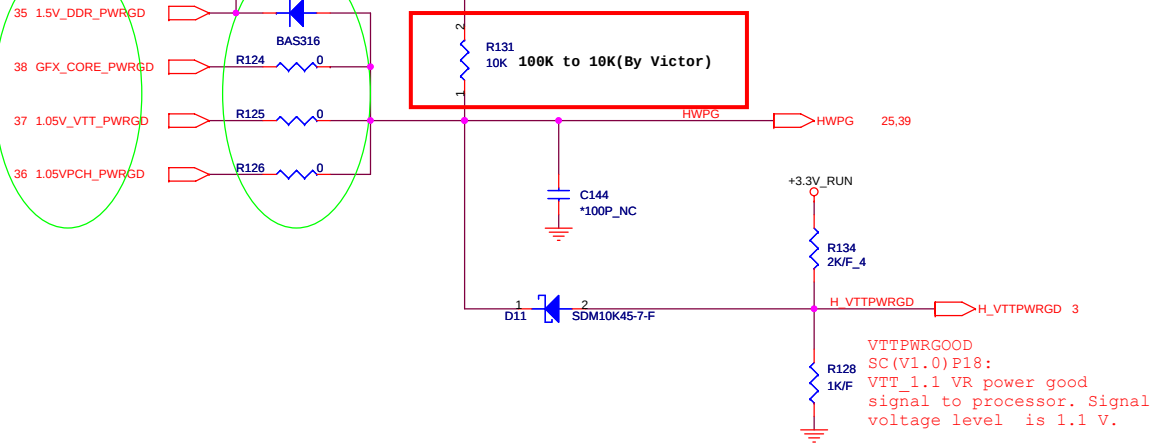


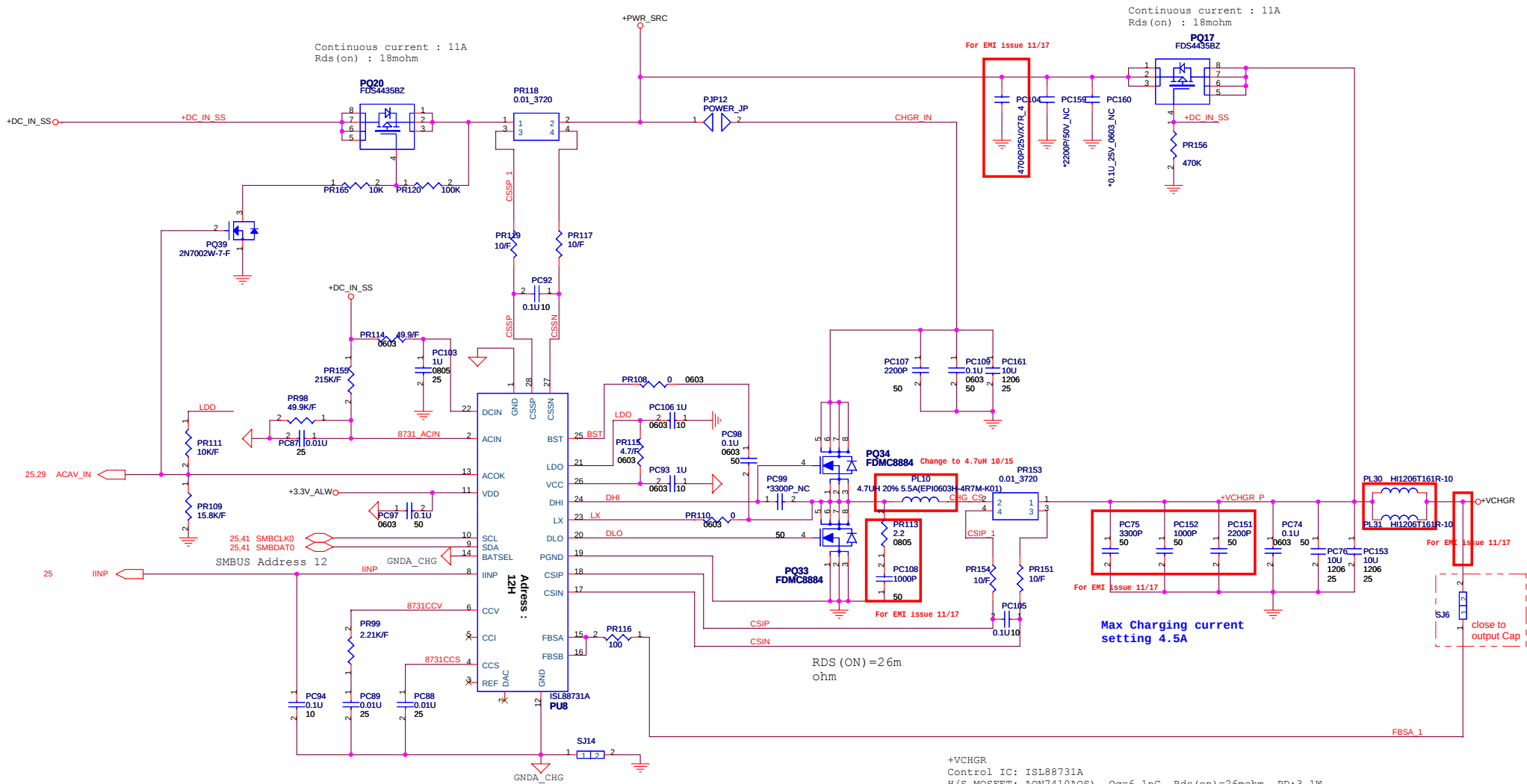
[illegible]

+3.3V_RUN ○ R130 2 1 10K THERM_ALERT#

SYS_SHD# ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77 'C	83 'C	89 'C	95 'C	101 'C	107 'C
6.8K	78 'C	84 'C	90 'C	96 'C	102 'C	108 'C
10K	79 'C	85 'C	91 'C	97 'C	103 'C	109 'C
15K	80 'C	86 'C	92 'C	98 'C	104 'C	110 'C
22K	81 'C	87 'C	93 'C	99 'C	105 'C	111 'C
33K	82 'C	88 'C	94 'C	100 'C	106 'C	112 'C

Check PWRGD Voltage





+5V_SUS
Fs=200K
TDC : 7.8A
OCP : 11.1A

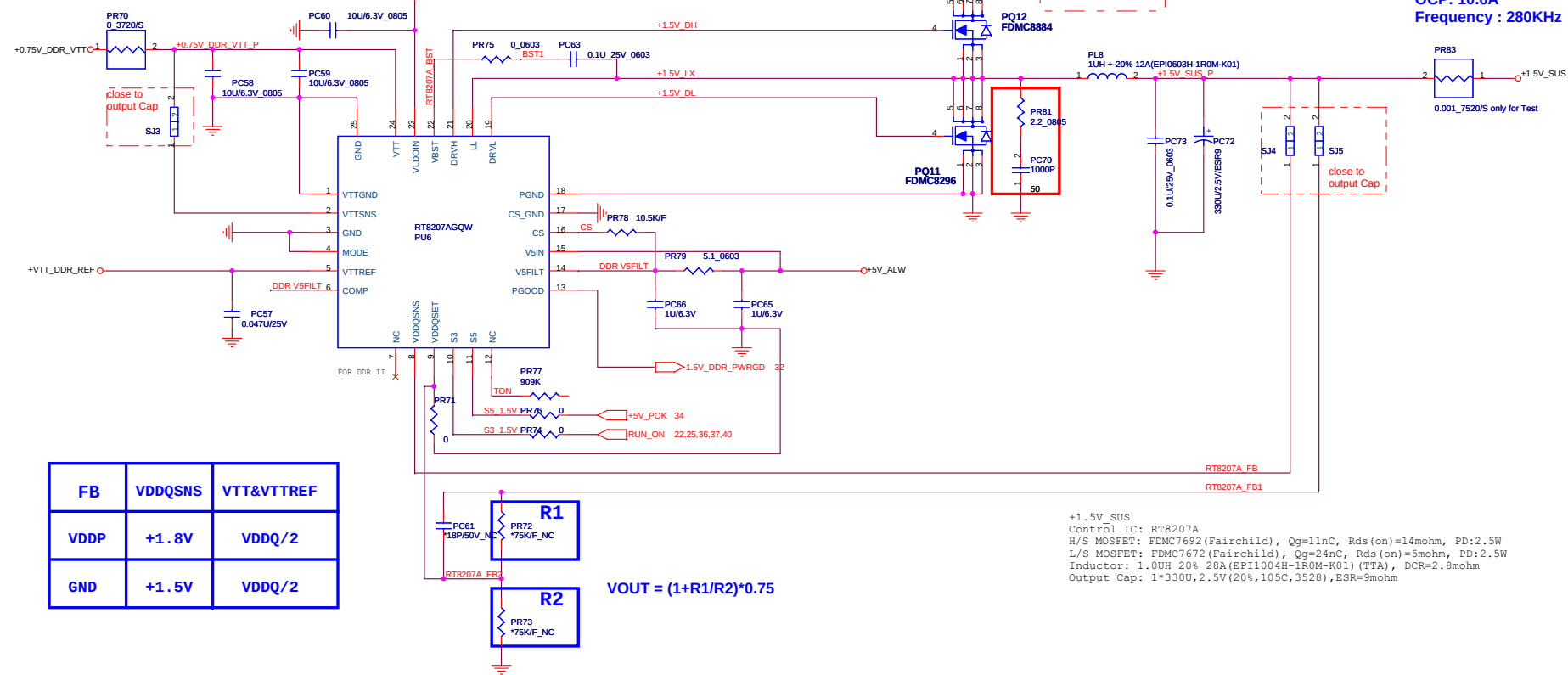
+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884 (Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296 (Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
Output Cap: 1*330U, 6.3V (20%ESR17,7343)

+3.3V_ALW
Fs=250K
TDC : 6.38(UMA) ; 7.6A(DIS)
OCP : 9.11(UMA) ; 10.9A(DIS)

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884 (Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296 (Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
Output Cap: 1*330U, 6.3V (20%ESR17,7343)

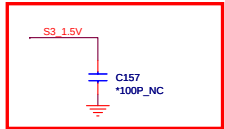
Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

+0.75V_DDR_VTT
TDC : 0.7A

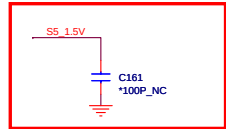


FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

$$VOUT = (1+R1/R2)*0.75$$

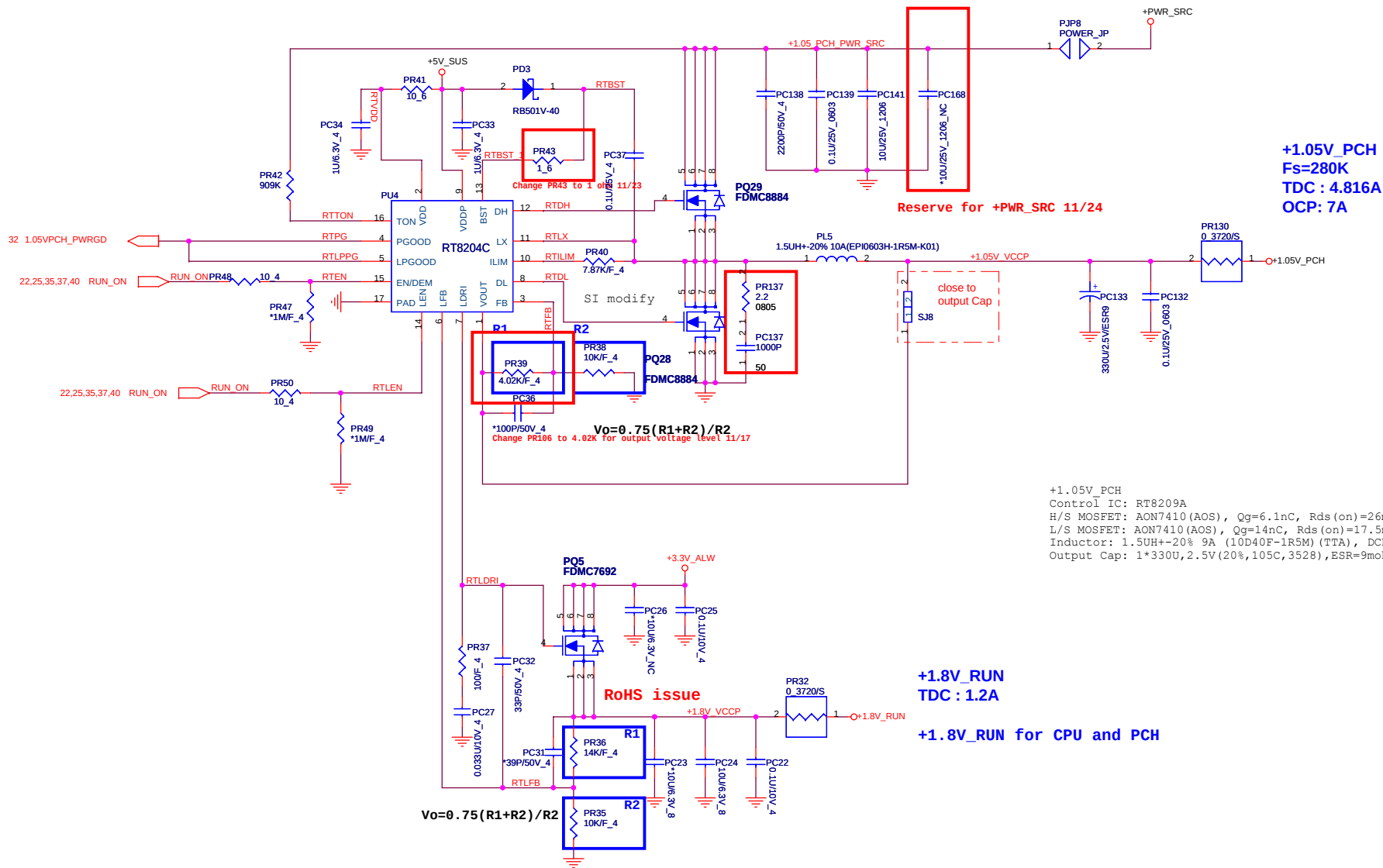


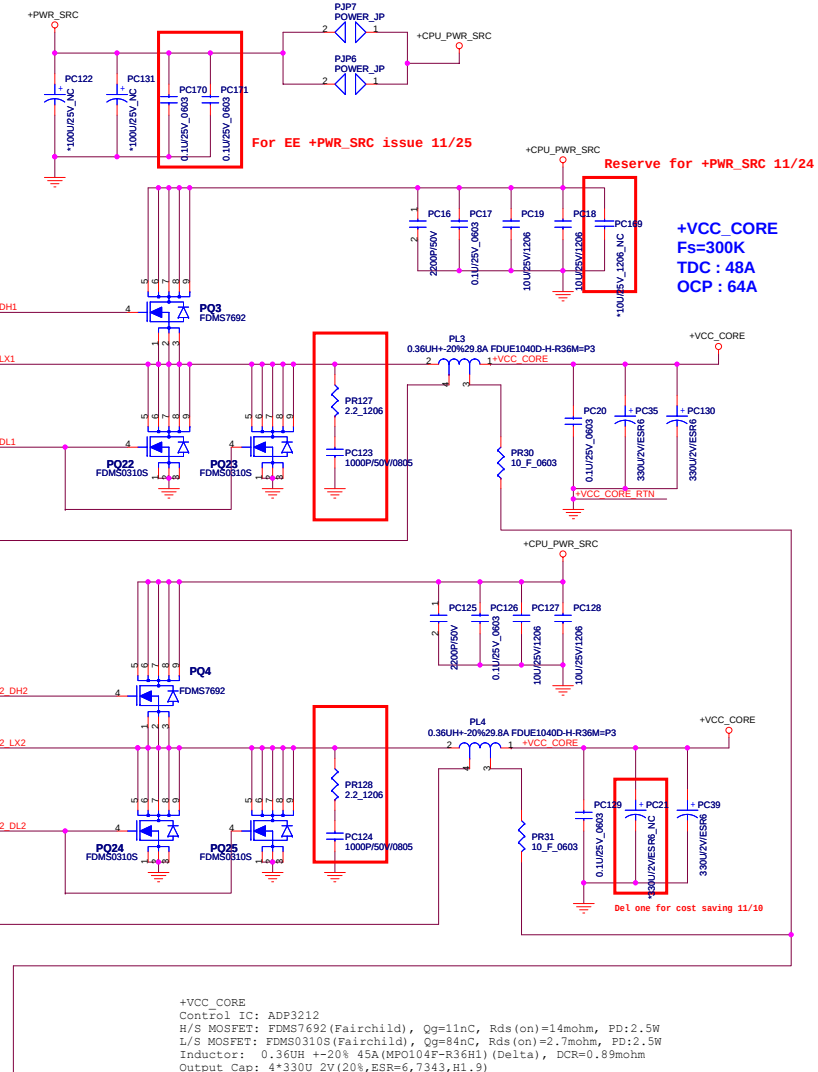
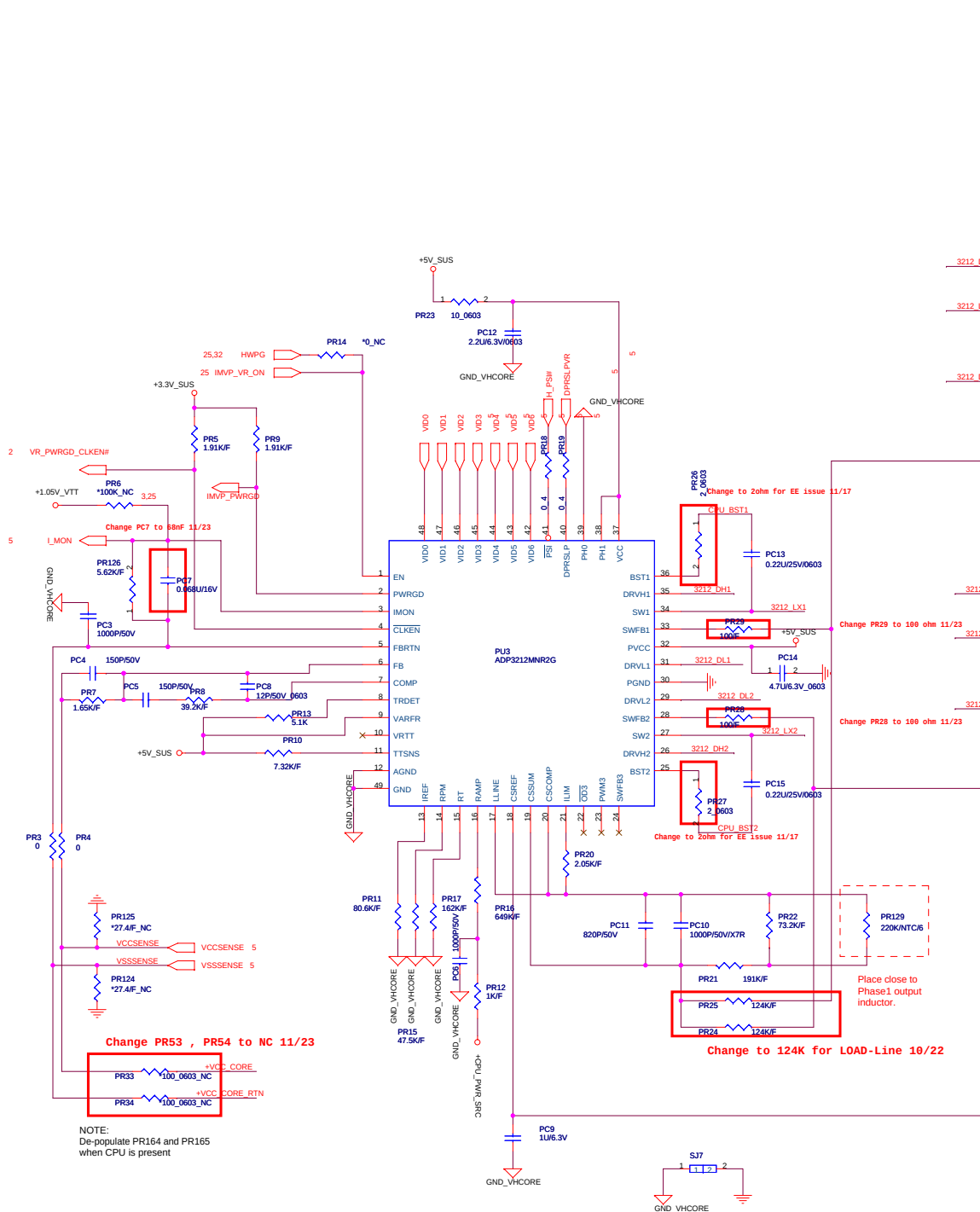
close to PR56



close to PR55

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMC7692 (Fairchild), Qg=1nC, Rds(on)=14mohm, PD=2.5W
L/S MOSFET: FDMC7672 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD=2.5W
Inductor: 1.0UH 20% 28A (EPI1004H-1ROM-K01) (TTA), DCR=2.8mohm
Output Cap: 1*330U, 2.5V(20%, 105C, 3528), ESR=9mohm





Change to RUN_ON

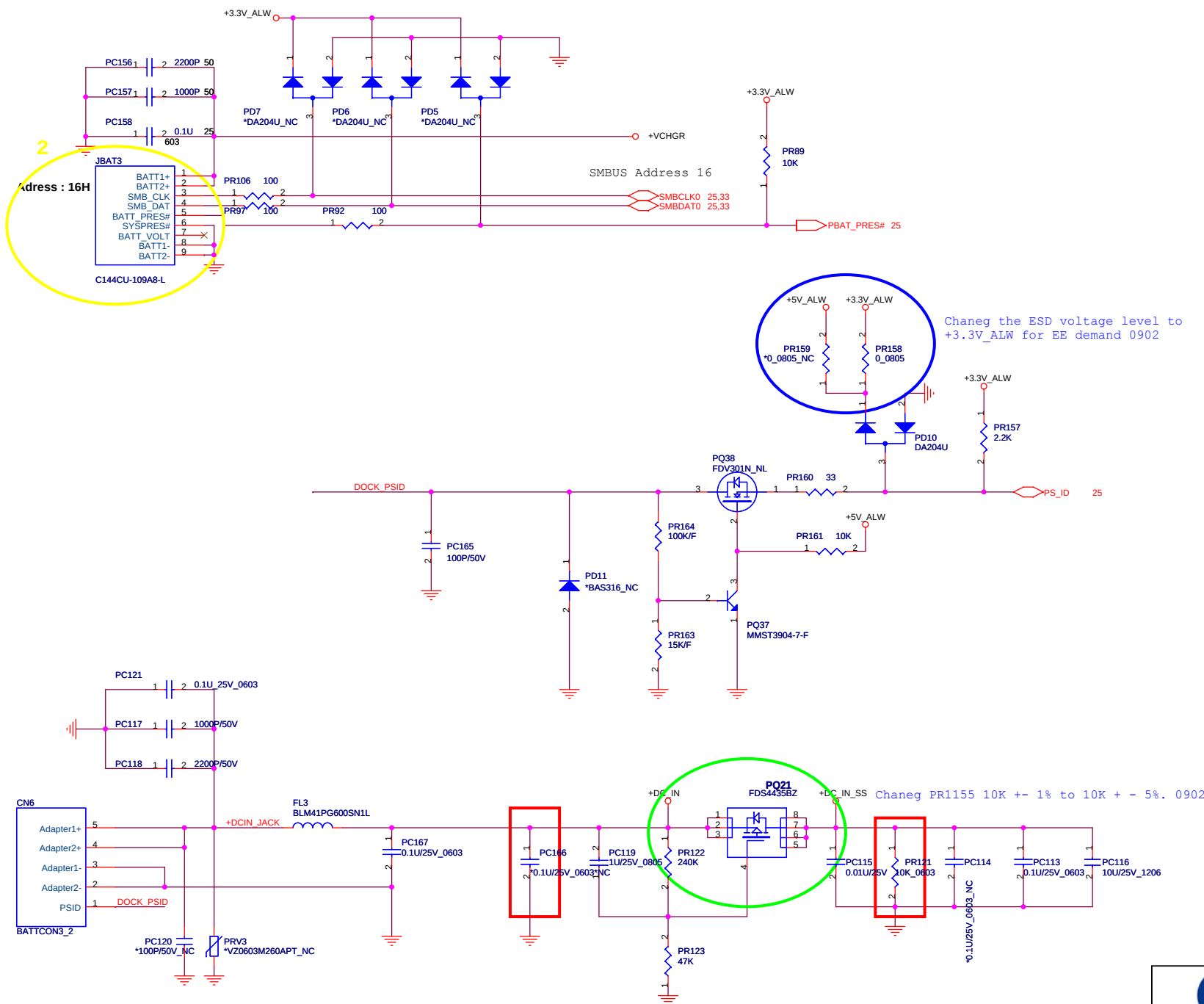
22,25,35,36,37 RUN_ON

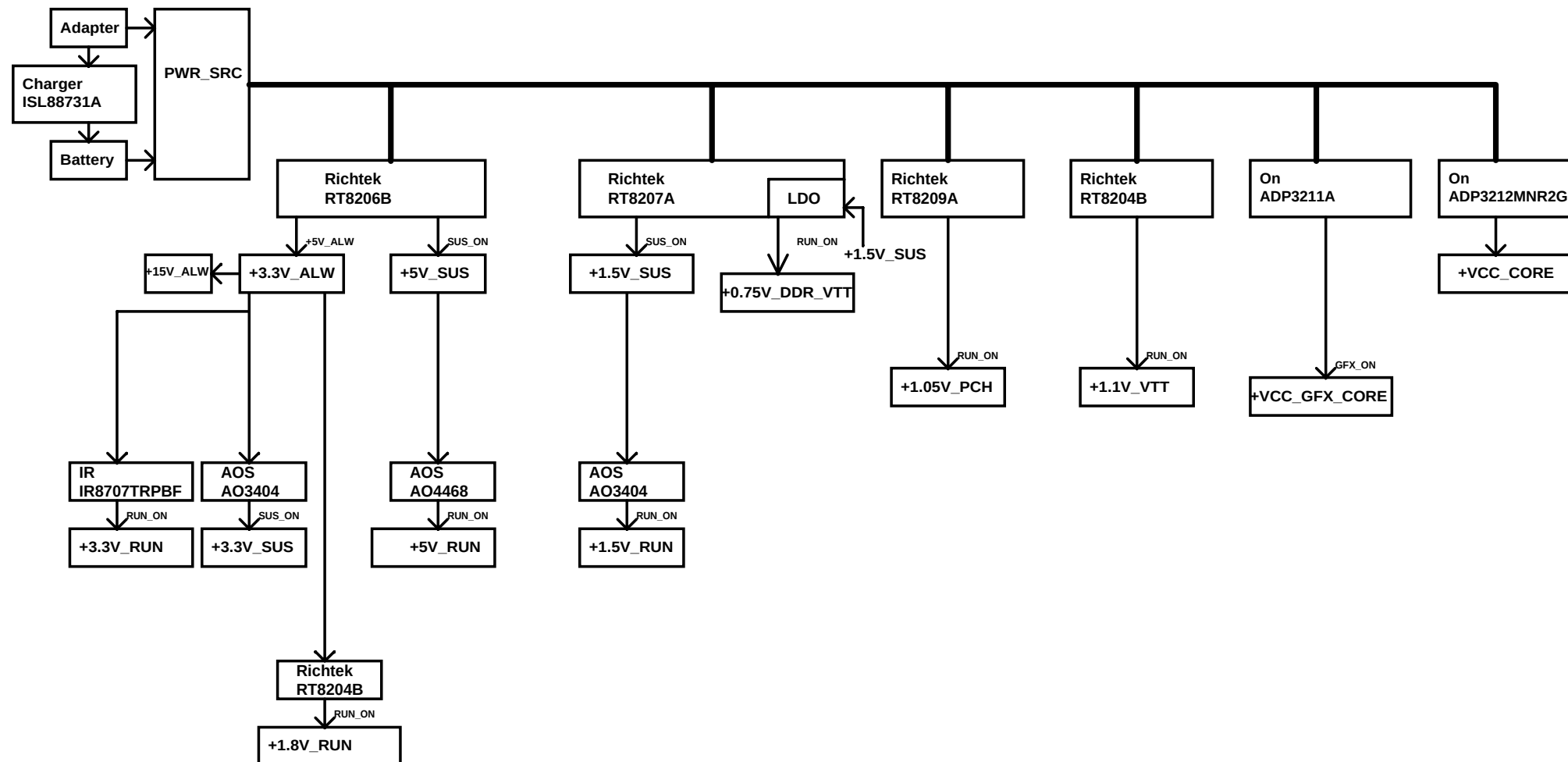
+5V_RUN
TDC : 5A

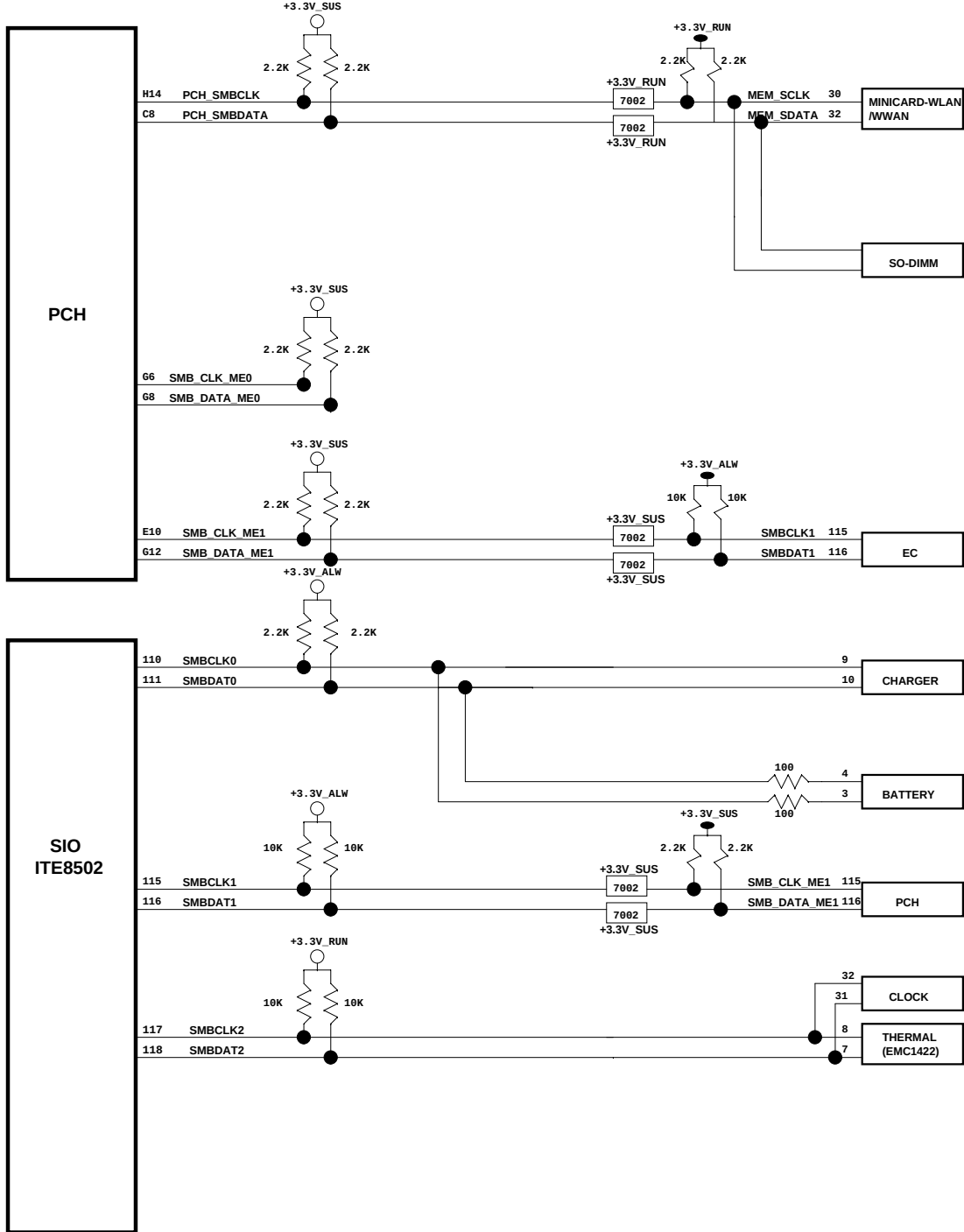
+3.3V_SUS
TDC : 0.26A

+1.5V_RUN
TDC : 0.35A

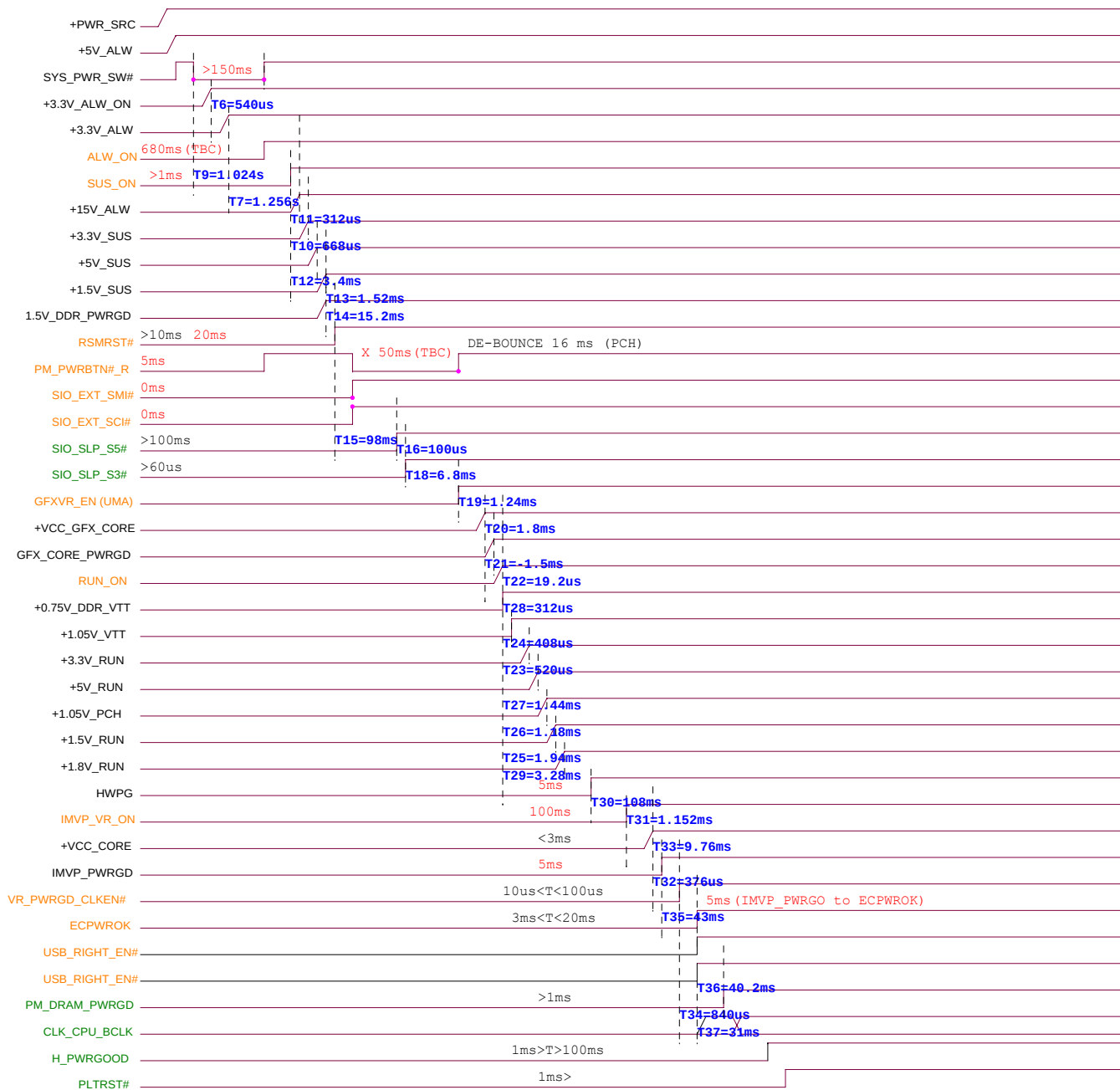
+3.3V_RUN
TDC : 4.9A







UM8_X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



Power Design Block Diagram

